CALCE NEWS

The Computer Aided Life Cycle Engineering
Electronic Packaging Research Center

January 1991 thru June 1997

A DTIC-Compiled Publication of CALCE
Newsletters from the University of Maryland

Scott, Frank

From: Joan Lee (Program Analyst)[SMTP:joanyuan@calce.umd.edu]
Sent: Tuesday, July 01, 1997 9:19 AM
To: Scott, Frank
Subject: Re: Placing Calce News in DTIC

From: "Scott, Frank" <fscott@dtic.mil>
To: '"joanyuan@calce.umd.edu"' <joanyuan@calce.umd.edu>
Subject: Placing Calce News in DTIC
Date: Mon, 30 Jun 97 15:09:00 EST

Joan, the DTIC Administrator, Mr. Kurt Molholm, received a copy of your newsletter and was thinking that you probably intended for it to go into the DTIC collection. Is that the case? If so, I'd like to download a number of issues from the www and make them available to our customer base--the DoD and their contractors. I'll need an e-mail from you saying it's OK. Thanks Frank Scott.

It is okay.

Joan Lee
(Program Analyst)
****

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CALCE News

January 1991

New Thrust in Cost Effectiveness of Electronics Designs

The topic of cost effectiveness for electronics packaging forms a major new thrust for the Center, added to the detailed technical issues that have been of primary interest heretofore. Prior physics of failure examinations, comparisons of predicted failures with those that actually occur, the great cost of the suggested techniques for improving reliability, and other background work indicate that many design features intended to improve the reliability of modern high quality electronics are largely obsolete and are now expensive and largely ineffective. In some cases, activities intended to improve reliability may degrade overall reliability by virtue of additional complexity at the system level. Technology of electronic components has improved dramatically but the reliability engineering visions have not kept abreast, and now in some cases are unintended hindrances.

As a result of this new direction, the Center has attracted several new sponsors, (shown at right) and there has been widespread interest from others. This newsletter contains several examples of the progress already being made by the Center. The subjects span several established engineering fields, all of which must be incorporated to develop the new criteria and speed its introduction into widespread usage.

It appears that we are in for some exciting times.

Summaries of Recent Significant Technical Activities

Reliable IC Package Design Guidelines Contract with RADC

A 24 month contract was awarded on June 1, 1990, to the CALCE Center to develop design guidelines for the materials, dimensions, and construction and assembly processes used in microelectronic packaging which will enable the user to design packages suitable for specific end-use environments. A potential list of the inputs required for the development of the design guidelines, including failure modes/mechanisms, package types, package elements, loading conditions, and assembly process conditions has been prepared. Also, variabilities in architecture, materials, manufacturing, testing and screening for each of the package elements are being documented. For additional information, contact Dr. D. Barker, (301)-405-5264.

Solder Fatigue Damage Project with NASA, Goddard Space Flight Center

The CALCE Center was awarded a research grant by NASA- GSFC, during the 1990-1991 year to analyze the inelastic strain history in a special solder fatigue specimen designed by NASA and UNISYS engineers for comparing the Low-Cycle fatigue properties of different solder compositions under thermal cycling. CALCE researchers are using nonlinear finite element methods to generate complete strain and stress history in the specimen, including detailed instantaneous partitioning between the elastic, plastic and creep components of strain in the solder. The purpose of the partitioning is to enable the use of more accurate fatigue damage laws. This is the first study in the literature where such partitioning has been attempted numerically for solder material. Nonlinear viscoplastic constitutive laws for the solder were obtained for this analysis from the literature and are being verified currently by NASA- GSFC engineers through detailed experiments. CALCE researchers are also working with UNISYS engineers in designing and conducting the fatigue experiments. For more information, contact

failure in similar temperature can be directly related to parameter drift, premature aging, and even catastrophic failures."

"Absolute temperature is often judged to be the culprit of device failures, and blaming absolute temperature may shift emphasis away from actual design or manufacturing deficiencies. In some cases, where temperature may be identified as an important ingredient in the explanation for unreliability, the product as designed is not suitable for operation in the desired environment without its being changed. Each action has its own costs, and the designer or user must fully understand the implications of each to produce cost effective reliable equipment. Understanding the role of temperature may be difficult even after close scrutiny."

"The data obtained and presented in this chapter indicate that: (1) the absolute temperature parameter is not as major a factor in microelectronic device failure mechanisms in equipment operation range of -55øC to 125øC (worst case junction temperature) as has been previously considered, and (2) the use of the Arrhenius temperature relationship as the dominant temperature acceleration model is not appropriate in this equipment temperature range. This model may have validity for failure mechanisms associated with wearout, but for the cases considered here, such failures occur well beyond the useful life of typical equipment."

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CALCE News

September 1991

Endurance Testing of Ceramic vs. Plastic IC in High Temperature and Humidity Environment Yields Important Results

An ELDEC team led by Lloyd Condra, with Steve O'Rear, Tim Freedman and Leo Flancia, and with technical assistance from Michael Pecht and Donald Barker of the EPRC, recently completed IC endurance studies to assess the possibility of replacing expensive ceramic IC packages with identical low cost plastic packages.

The study reveals that the ceramic package could be replaced by its plastic equivalent with no determinable effect on operational lifetime or performance but at significant cost savings to the customers. Portions of the report are excerpted below.

Circuit cards were assembled using both plastic and hermetic versions of a custom IC. These circuit card assemblies (CCA's) were compared against each other as well as against an older discrete version of the card, which had a history of reliable operation for over 20 years. The IC version of the CCA's were coated with either urethane or parylene, and along with unassembled IC's, were tested for 1000 hours in 85øC-85% relative humidity with intermittent bias (tempera- ture, humidity, bias - THB). In addition, CCA's which had previously received 1000 temperature cycles between -55øC and 85øC were tested for up to 650 hours in 85øC-85% RH.

No differences in parametric outputs or failure rates were observed between plastic-encapsulated and ceramic versions of the components in temperature-humidity-bias (THB) environments and in combinations of THB and temperature cycling. Using the best available acceleration models for THB, the expected lifetime of plastic and ceramic components in avionics operating environments is estimated conservatively at over 20 years. It is concluded that, in this and similar applications, there is no reliability differences between plastic and ceramic IC's due to temperature-humidity.

Tests were also conducted for cards conformally coated with urethane and parylene, containing both plastic and hermetic IC's. From our tests, it appears that the cards coated with urethane are in the wearout stage, while those coated with parylene are still in the useful life stage. Since these cards had been temperature cycled prior to collection of the data shown here, we believe that the 1000 temperature cycles of -55øC to 85øC took the cards to the end of their useful life, and they began wearing out in THB. By contrast, the parylene-coated cards had significant useful life remaining at the start of THB (although half of them had failed by the end of THB). It is thus at least a preliminary conclusion that circuits coated with parylene are more reliable than those coated with urethane.

An Alternative Wire Bond Test

Wire bonds in microelectronic packages either connect the bond pad to I/O lead wires, or connect two bond pads (i.e. in multichip modules). To determine the quality of the fabricated bond, MIL-STD-883C specifies a non-destructive bond pull test, whereby an apparatus having a hook-shaped member is utilized to hook onto and pull each bonded wire with a predetermined force. The wire must be able to withstand this force to be acceptable. With bond wire spacing approaching 0.006 inches, placing the hook of the testing apparatus around a single bond wire without damaging adjacent wires is difficult and

tedious. Besides, such bond pull test can potentially result in misleading conclusions. For example, the hook may slip to the highest portion of the loop resulting in a peel mode of failures giving a lower bond pull value. Elongation of the wire material also effects bond pull test results.

An alternative bond test method being investigated at the Center involves placing the wire bond in a magnetic field and passing an alternating current though the wire causing it to fail under repeated flexure. J.I. Tustaniwskyj, R.J. Usell, and S. Smiley of UNISYS Corp., who hold a patent on the technique, have loaned the equipment to the Center, and a set of unique test fixtures, each with 512 wirebonded interconnections, have been loaned to the Center by Westinghouse. The test procedure involves placing the test coupon in a magnetic field and passing an alternating current through the wires. The magnetic field and alternating current excite motion in the bond wire to arrive at fracture-fatigue failure information.

The test can be used as an in-line non-destructive test technique, in which the wirebonds on a test fixture can be tested at regular intervals to ensure that the manufacturing process is under control. The technique can also be used as a life test evaluation method.

EPRC and Westinghouse Collaborate on AWACS Project

Experiments on forced convection cooling of printed circuit boards are being conducted at the Center as part of the Westinghouse AWACS project. Experiments involve a test structure whereby the thermal profile of multiple circuit cards can be investigated in terms of card separation, component placement, and flow variations. A 10" 12" infrared window is being utilized so a complete thermal profile can be obtained. So far, empirical correlations characterizing the thermal behavior of circuit boards for different power levels and air velocities have been determined. Selected results were presented in the open forum of the ASME National Heat Transfer Conference at Minneapolis, Minnesota on July 28-31, 1991.

Litton - EPRC Plated-Through-Hole Study

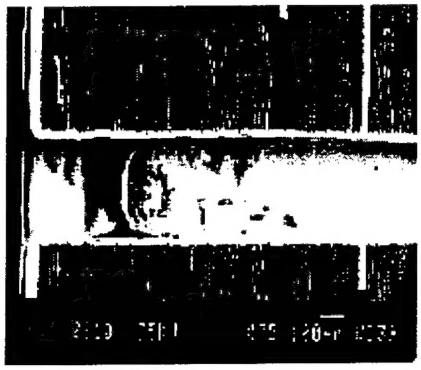
Navin Bhandarkar, Dr. Abhijit Dasgupta and the programming staff of the Center are completing an effort in collaboration with Litton-Amecom, College Park, MD, to optimize aramid PCB designs for reliability and producibility. Litton-Amecom had noted early failures of PTH when Kevlar (aramid) reinforced boards were used for high density surface mount PCBs. This failure was attributed to mismatches of coefficient of thermal expansion (CTE) between the Kevlar and PTH plating in the thickness direction. A test program has been initiated by Litton-Amecom to optimize PTH design, involving the manufacture of design verification boards (DVBs) with several different configurations of PTHs by four board vendors. The purpose of the study is to determine the effect of the following variables on PTH life:

- Hole Diameter
- Board Thickness
- Plating Thickness
- Nickel Overcoats
- PTH Plating Properties
- Pad Diameter
- Position, Quantity, and Size of Non-Functional Pads Thermal Cycling Profile

Simultaneously, EPRC has started computer simulation of the DVBs by modeling the various PTH configurations using finite element analysis. The total life of the PTH in the computer simulation is broken down into fatigue crack-initiation life and fatigue crack-propagation life, with cyclic stress/strain amplitudes obtained from the finite element model for the given thermal cycling profile.

PTH life predictions based on the software simulation show excellent correlation with measured PTH life. The site of the peak strain range (a failure indicator) in our simulations coincides exactly with the observed failure sites in the experimental specimens. The life predictions for different plating thicknesses and PTH aspect ratios are within 10% of experimental observations. Further, the changes in

PTH life with variations in geometry follow similar trends. The real strength of the simulation lies in the ability to study parameters that are either difficult to build into the board or were not built in during the original design conceptualization phase. Examples of parameters that are expensive to study experimentally include the effect of board CTE and upper plating properties on PTH life. Simulation provides an ideal design tool in such situations. The results from this study are being incorporated into an upcoming revision of the PTH software program to be distributed to our members. With this revision, the PTH software will become one of the most comprehensive prediction models available.



This is a scanning electronic microscope picture of a cross section of a failed PTH. Failure occurred at a location and a manner predicted by the Center analysis.

Diamond Heat Sinks For Advanced Packaging - Investigations with LPS

The EPRC Microelectronics Device Lab is currently working on a joint project with the Laboratory for Physical Sciences (LPS) to improve IC thermal management by introducing diamond substrates. In the conventional packaging, the semiconductor chip is directly attached onto the packaging substrate (ceramic in this case) by an adhesive. Due to the low thermal conductivity of the packaging materials, the heat dissipation through the package is poor. The localized high temperature at the heat sources (normally the junctions of transistors) can cause electrical failures. The heat dissipation is expected to be greatly improved if a thin layer of diamond is coated on top of the packaging substrate owing to the high thermal conductivity of diamond (~10-12 W/cm K). Thus the generated heat can be immediately carried away to the entire substrate area, rather than being accumulated in the vicinity of the heat sources. Other candidate substrates of interest to the Center include Silicon Carbide and Aluminum Nitride.

The temperature measurement technique is an important element of our effort to qualify new substrates. As part of the LPS led effort, EPRC is applying infrared microscopy in order to obtain accurate three dimensional thermal maps. The infrared data is then correlated with the EPRC thermal models and with temperature distributions obtained using electrical diode sensing.

Boeing Commercial Airplanes Group Funds Expanded Effort to Develop An Improved Design Model for Electronic Packaging

There has been strong interest in broadening the CALCE Software to include a new basis for design reliability activities. With the conclusion that Mil-Hdbk-217 should not be used as a design tool, and the strong evidence that the temperature models expressed by the Arrhenius equation are inadequate, a new approach is needed. In studying their needs, Boeing is now funding two new reliability activities to fit into the design process. The first is the Design Integrity Model, which is the extension of the CALCE Software, but with all of-217's influences replaced with scientifically based physics of failure models. This model will include a temperature cycling failure mechanism as well as a steady state temperature failure mechanism. The second, Design Validation and Process Verification, is based in the concept of expanded use of environmental stress screening (ESS) resources. Combining the failure trend analyses

from the Design Integrity Model with the use of ESS resources, provides a design model validation step. Expansion of those same resources for process verification will provide a degree of confidence that the manufacturing processes do not create inadvertent sources of failure sites.

Boeing is encouraging other interested companies to help co- sponsor this activity. Charles Leonard at Boeing can be reached at (206) 477-0278 for further information.

Center Research on Reliability of MMICs

Microwave monolithic integrated circuits (MMICs) are realized by fabricating passive and active devices on a common semi- insulating substrate such as Gallium Arsenide (GaAs). Today, GaAs MMICs have become important in microwave communications and high frequency measurement systems because of the potential for a high level of integration, diversity of circuit function, and extremely wide bandwidth. Among the remaining critical issues for GaAs MMICs, is the reliability of the active and passive elements.

The MMICs currently investigated in the Microelectronics Device Lab of EPRC include Texas Instruments (TI) 96214 power amplifiers, L-band power transistors, field-effect transistors (FETs), and high electron mobility transistors (HEMTs). The electrical measurements are conducted at desired temperatures to monitor degradation of device performance. Failure criteria are usually defined as a certain percentage decrease in gain or the source-to-drain saturation current, I_{dss}.

The EPRC's microanalysis equipment allows for the analysis of most electronic failure mechanisms. For example, metallization damage is examined by scanning electron microscope (SEM) techniques, while the energy dispersive X- ray analysis (EDXA) provides compositional analysis of electromigration - enhanced interdiffusion at metal / semiconductor contacts (one of the principal causes of active device failure). Thermal analysis is also conducted and temperature distributions over the device surfaces are obtained using an infrared microscope during device operation with junction temperatures and hot-spot locations identified to within 0.1øC, with 15æm resolution. The CALCE V3.0 thermal modeling software provides a computer simulation of the heat transfer process and is being modified to furnish an alternative approach for lifetime prediction.

Collins Avionics and EPRC Study Cathodic- Anodic Filament (CAF) Growth

The study of cathodic-anodic filament (CAF) growth by Collins Avionics and EPRC is a topic which addresses a "dendritic-like" growth between traces on printed wiring boards at high relative humidity and high voltage bias. In order to investigate this problem scientifically, Collins and the EPRC have cooperatively begun a set of experiments to test for CAF. The goal is to provide guidelines on trace spacing versus voltage bias for various printed wiring board materials. Traces on both inner and outer board layers are being tested.

Investigations Into the Effects of Temperature Continue With Phase II Support

A Phase I study into the effects of temperature, funded by the US Army, Fort Monmouth, is complete. The study concludes that the view of steady state temperature as the significant failure accelerator can be misleading, since the effects of temperature are not accurately modeled by exponential relationships such as the Arrhenius equation. A more realistic view of temperature's influences would include temperature gradient effects and the effects of transients as they affect electrical, chemical and mechanical stresses. Fatigue failure seems to be a more important effect of temperature, due to gradients, transients and cyclic ranges rather than temperature itself.

A Phase II study has been authorized, also by Fort Monmouth, to assess temperature related design

rules, screening procedures, and acceleration factors currently in use for IC's operating in the temperature range of -55 to 125øC. An experimental verification effort will also be conducted to address package related failures. A portion of the research will be conducted through visits and cooperative programs with various companies involved in the manufacture of integrated circuits as well as OEM's. The visits will involve presentation of the state of the art in temperature dependence of microelectronic devices, outlining the dominant failure mechanisms in the temperature range of -55øC to 125øC. Finally, we will be developing guidelines for the effect of steady state temperature and changes in temperature on microelectronics. A workshop will be held at the University of Maryland on "Temperature Dependence of Microelec- tronics", in the latter part of 1992.

The EPRC Performs Vibration Test and Simulation of Advanced Circuit Boards for General Dynamics

Kent Bennett of General Dynamics (GD), Fort Worth Division spent several days in early July helping the EPRC in analyzing and testing advanced circuit board configurations. Experiments were performed on five different circuit boards and the results were compared to those produced by the CALCE Software module. The boards provided were multi-layer boards of pin- in-hole and surface mount variety representing a wide range of configurations used in GD avionic systems such as: heat rails, stiffener ribs, connectors, unsymmetric clamps, and wedgelock card guides. Dr. Donald Barker, co-director and resident vibrational analysis expert of the Center, discussed ways in which CALCE V3.0 software could be used to model circuit boards with non-standard constructions and geometries.

Characterization of Packaging Materials

One of the crucial problems encountered in the design and reliability modeling of microelectronic devices is the shortage of reliable data on mechanical, thermal and electrical properties of microelectronic materials such as die materials, ceramic substrates, conductive epoxies, solder, thin coating materials, and composite board materials. The ability to quantify the behavior of materials over a range of temperatures and strain rates is critical for microelectronic package design. This lack of information is partly due to the difficulty of characterizing these materials at the extremely small length scales commonly encountered in microelectronic packages. A major aspect of modern materials science is the quantitative characterization of microstructure and exploration of the relationship between microstructure, processing and properties, using both mathematical models and experimental measurements.

The EPRC is now in the second year of a program geared to collect properties of all electronic materials from different sources, and establish a Material Database Management (MATDM) system which possesses multiple functions to serve electronic design engineers and researchers. For materials whose properties are not completely available, mathematical modeling of microstructure and appropriate testing is being conducted at the Center. The program is aimed at investigating the fundamental failure phenomena of commonly used materials at different temperatures and environmental conditions. Detailed mathematical modeling of the micro- structure and appropriate testing will define the linear and nonlinear thermal, thermo-mechanical, electrical and magnetic constitutive properties of electronic materials. Studies of mechanical properties include damage properties such as fracture toughness, fatigue crack initiation, crack propagation under cyclic stress conditions, creep deformation and rupture at high temperature and creep fatigue interactions. This program is aimed at quantifying the statistical variability of material behavior, since variability can be a key reliability factor.

A series of material property tests have been conducted on GaAs wafers, glass-epoxy, glass-polyimide, GF laminate, kevlar-polyimide, stycast 2651 MM FR with catalyst 9, stycast 2651 MM FR with catalyst 11, and Norbak 148/27. The critical material properties tested include modulus of elasticity, Poisson's ratio, ultimate strength, fracture toughness, coefficient of thermal expansion, and thermal conductivity. The tested material properties are stored in the Center material data base-- MATDM, which is utilized by the CALCE V3.0 software.

Handbook of Electronic Package Design

This reference text discusses the electronics design process in- depth and examines techniques for microelectronic packaging, as well as fundamental topics in the development of a complete electronic system, including:

- techniques for the design and fabrication of microelectronic packages
- board fabrication steps, from bare substrate formation to machining, metallization, and preparation for component mounting for organic and ceramic printed wiring boards
- methods used to predict and measure the stresses of electronic systems in service and assess and maximize reliability
- tools for designing against thermal and mechanical damage and failures resulting from monotonic and/or cyclic thermomechanical loads, excessive vibration and/or shock, and corrosion

This book is available from Marcel Dekker, Inc. Call 1-800-228-1160 to order.

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CALCE News

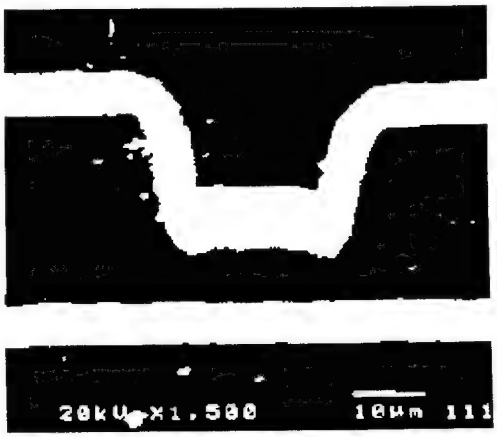
January 1992

Investigation of Potential Failure Mechanisms of HDI Packages

EPRC is currently investigating the potential failure sites and failure mechanisms of overlaid high density interconnects (HDI) due to humidity cycling. Overlaid HDI is a new interconnect technology developed by GE with very promising reliability, packaging density and electrical performance advantages. Interconnection between chips is accomplished by overlaying multi-layered metallization/ dielectric. However, as a new technology, it is important to understand potential risks and to develop tailored quality assurance and qualification procedures. Novel potential failure mechanisms include de-lamination, metallization and dielectric layer voiding, metallization and dielectric layer buckling, corrosion of metallization, and electromigration.

To address the potential failure mechanisms of HDI, we found that a thermal cycling stress alone could not induced failures in a short time. The reason may be that the compliance of the layer material requires a large thermal cycle to induce material property changes at the temperature extremes. On the other hand, because the ceramic is not hydrophilic, high moisture content of the dielectric layer induces a "swelling" mismatch which can be damaging. Furthermore, the properties of polyimide are dependent on relative humidity in that the dielectric constant increases about 35%, dissipation factor increases by about a factor of 3, and breakdown voltages decrease from 3.3 MV/cm to 1.6 MV/cm when relative humidity changes from 0% to 100%; and the adhesion strength of polyimide to silicon and Al2O3 decreases with increasing water absorption.

The SEM micrograph below shows a cross section of an HDI package around a via before humidity cycling. The sectioned HDI device was subjected to humidity cycling (40% - 90%) at 30øC and the effect of humidity cycling is being examined with SEM. A finite element method was used to predict stress distribution under operational load. Nonlinear viscoelastic constitutive analysis and nonlinear buckling analysis is being formulated.



SEM micrograph of a cross section of the HDI around a via.

Physics of Failure Based Package Compiler Software for Design and Reliability Assessment

The EPRC has begun developing software for reliability assessment and design of microelectronic packages. The software is based on the results of a two year effort, supported by the Air Force Rome Laboratories, to develop design guidelines for microcircuit packaging. The software incorporates physics of failure models relating life predictions to mechanical, thermal, electrical, and chemical stresses, material properties, and geometric configurations. In addition to its design capability, the software presents an alternative to MIL-HDBK-217, and will serve as a valuable aid in qualification and quality assurance.

Our approach was to model generic package elements including: die, die attach, substrate, substrate attach, wirebonded interconnects, tape automated bonds, flip-chip bonds, high density interconnects, cavity-type and plastic cases, leads, lead seals, and lid seals. A set of synthesis tools then form these elements into structures such as hybrids, or multi- chip modules. Databases with candidate materials and their properties aid the design process and provide data for the reliability assessment. Operational and environmental conditions can then be selected or specified. Once dimensions, materials, and environments have been input, potential failure mechanisms and modes are analyzed, ranked and an estimated average time to failure is reported. In addition, design inconsistencies are presented as warnings in the final output. If the estimated reliability does not fulfill mission requirements, the designer can evaluate alternate designs, in order to optimize to a cost effective microelectronic package.

Course ENME 808P: Microcircuit Manufacturing and Reliability

The University of Maryland is offering a new graduate course titled Microcircuit Manufacturing and Reliability (ENME 808P). This course relates manufacturing processes to reliability and performance of microcircuits up to the component level, including analog and optoelectronic components. The key aspects of manufacturing yield, defects and reliability will be taught. The information presented will cover material science, mechanical and electrical behavior from the die level to a packaged device. The new text used for this course is Dr. A. Christou's book titled Reliability of Monolithic Microwave Integrated Circuits, John Wiley, 1992.

Connector Reliability Modeling

In close coordination with AMP Inc, a leading connector manufacturer, CALCE EPRC is developing a mathematical model for determining connector reliability. The model is based on the physics of the contact interface as a function of exposure time and load for specific failure mechanisms.

AMP is providing the EPRC with data from Class III IMFG tests conducted on phosphor-bronze specimens with a 50 æ CoAu plating on a 50 æ nickel underplate. The Industrial Mixed Flowing Gas (IMFG) test is an accelerated environmental test applied to study the effects of various environments on the corrosion of metals placed in these environments. The Class III environment represents a typical industrial location where moderate amounts of pollutants and particulates are present in poorly controlled environments. The data consists of contact resistance as a function of load for various exposure times.

The classical resistance law consisting of a constriction and film resistance was used in the model development. However, the developed model also incorporates environmental conditions, all in a mechano-stochastic manner. The developed model thus has applicability for determining the probability of obtaining a contact resistance as a function of load for different environmental aging classes.

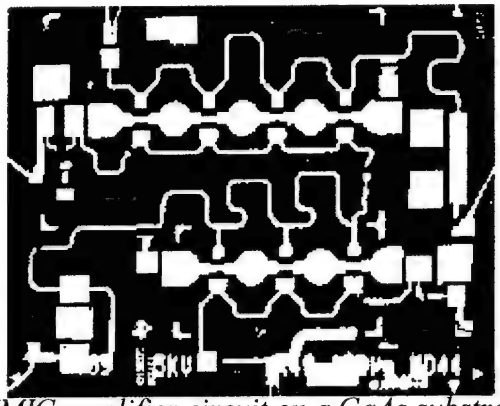
The model is also valuable in two other ways. If a maximum design resistance is specified along with a desired confidence level, then we can determine either the maximum acceptable aging or the required minimum load. This approach provides a major advancement to those methods given in MIL-HDBK-217 which are more than 20 years out of date for modeling connectors.

EPRC is now in the process of analyzing AMP data from the Class II IMFG test in order to enhance the developed model. At a recent meeting at AMP, other factors affecting connector reliability such as wear of the contact finishes and stress relaxation in the spring material were also discussed for study and incorporation into the model.

Manufacturing Qualification, Design and Reliability Testing of Analog Integrated Circuits on GaAs

This DARPA funded project at the University of Maryland CALCE EPRC has as its objective the

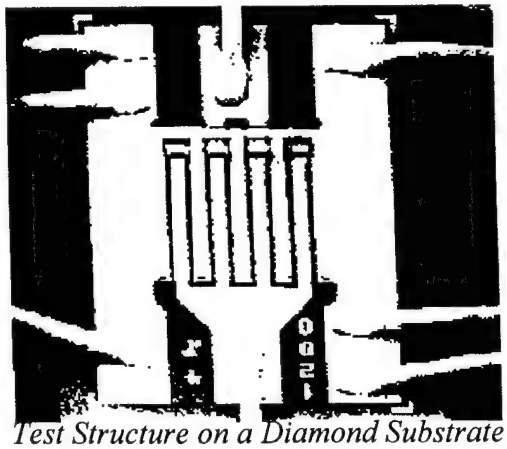
understanding of basic failure mechanisms of monolithic microwave integrated circuits. Reliability analysis has concentrated mainly on circuits obtained from Texas Instruments, Raytheon, M/A- COM and Hughes Aircraft. The Center research team, led by Dr. Aris Christou, has concentrated on generic failure mechanisms and has separated the effects according to frequency. The physics of failure model treats each of the failure mechanisms related to passive and active components as independent variables. The test results to date indicate that at L-band frequencies, a cross coupling term exists between active and passive components, while at higher frequencies the failure rate of passive components becomes negligible. The study also includes a thermal transient analysis of MMIC package configurations. In a pulsed environment, transient thermal and electrical effects are important. The finite element study has indicated that buckling of the passivation may occur as well as the occurrence of micro-cracks in the microstrip circuit. The new investigations will concentrate on the high frequency amplifiers from Hughes Aircraft. Generic codes developed as part of this project will enhance industry's competitiveness in the manufacture of analog circuits.



MMIC amplifier circuit on a GaAs substrate

Diamond Substrates for Low Cost Packaging

This joint project with LPS has as its objective the understanding of thermal-spreading properties of diamond and diamond films in a heat sink application for high density packages. Diamond films supplied by LPS may be used in high-end computer products to dissipate heat from high power semiconductors. In a computer application, improved diamond heat sinks enable microchip designers to pack circuit chips tighter without the danger of overheating. The new diamond heat sinks presently being analyzed by the Center will also make it feasible to use shorter wavelength lower efficiency lasers for communications. The Center experiments have concentrated on thermal impedance measurements on test circuits where the power dissipated has been previously determined electrically. The test structures will also become a standard technique for power dissipation measurements and for diamond heat sink qualification.



Test Structure on a Diamond Substrate

Although diamond heat sinks are perceived as high cost heat sinks, the developed thin film substrates will only cost additional fraction of pennies and a batch processing computer integrated manufacturing CVD system is presently available from original equipment manufacturers (OEMs). Dr. Christou has also completed a preliminary cost-benefit analysis for diamond substrates and has indicated that the future emphasis for diamond substrates must be placed on the manufacturing science. In this respect, we are looking for participation in the formation of a special industrial consortium for diamond at the level of $25K per company. All interested companies are encouraged to discuss their interests in this program with Dr. Christou.

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CALCE News

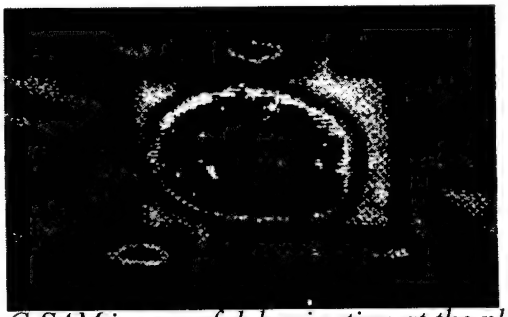
August 1992

Plastic Package Effort

Under the sponsorship of several CALCE members, a major effort has been undertaken on the key issues pertaining to the use and qualification of plastic encapsulated microelectronics (PEMs). The emphasis of the effort is on investigating the potential failure mechanisms which are unique to plastic packages, determining which of these failure mechanisms are "real" threats, developing a life-test procedure for the failure mechanisms, and developing guidelines for screening. The overall goal is to present a science-based perspective of the potential use, life testing and screening of industrially mature plastic packages.

Plastic packages have been used in commercial and industrial products for decades. As is well-known, they offer cost, availability, size, weight, performance and reliability advantages. Consequently, they have attracted strong attention for government and military applications. Although the major impediment to the use of plastic packages in this high reliability market has been the outdated "pi" factor for plastic packages in MIL-HDBK-217, MIL-STD-883 and MIL-M- 38510 procedures and test methods for screening packages need also be updated. What is required is a non-destructive on- line, but tailorable, screening procedure for plastic packaged parts for use by QML manufacturers.

The CALCE EPRC has the capability to non-destructively evaluate plastic packages with a C-mode Scanning Acoustic Microscope (C-SAM). This technique is capable of detecting defects (crack and voids) in the encapsulant and die attach, and delamination of interfaces. We expect to develop a method to relate the C-SAM results to short and long term reliability of plastic packages. Several papers are planned on such topics as: the impact of plastic packages on performance, cost, reliability and availability; failure mechanisms unique to plastic packages; and screening and life testing of plastic packages. For more information, contact Dr. Michael Pecht at (301) 405-5323.



C-SAM image of delamination at the plastic/paddle interface

Thermal-Mechanical Properties of Flex Circuits

mechanical properties of flexible printed circuit (or flex circuit) which exhibit visco-elastic properties at operational stress conditions. Flex circuits are composite structures with a metal foil pressed between sheets of flexible dielectric joined together by an adhesive system. The project includes the investigation of thermo-mechanical properties under static and dynamic load conditions. Proper characterization of these properties is important as inputs to physics-based reliability and design models for flex substrates and related interconnections such as wire, traces, and connectors.

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CALCE News

January 1993

FEA Modeling For REL-TECH

The CALCE Electronic Packaging Research Center is continuing development of generic Finite Element Analysis (FEA) models that allow computation of thermal, thermo-mechanical, hygro-mechanical, and mechanical responses of Advanced Interconnect Technology (AIT) structures. This effort forms part of a joint NASA, Army, Navy, and Air Force Reliability Technology (REL-TECH) program to evolve a detailed understanding of reliability of AIT structures in space and military environments.

For the first phase of the program, three-dimensional global- local FEA models have been developed for the General Electric High-Density Interconnect (HDI) Multichip Modules (MCMs). The global model includes an entire substrate containing active elements. Coarse thermal and stress analyses are then automatically conducted to investigate potential failure mechanisms, such as substrate and die cracking. The results of the global analysis form boundary conditions for the local model which provide a refined analysis of vias, bond pads, metallization lines and material interfaces. Thermal and stress analyses from the local model are used for investigating failures, including fatigue of vias and metallization lines and deadhesion failures at various material interfaces. Constitutive models are being developed for nonlinear stress-strain and creep behavior of the thin film polymers used in these packages, using data generated from experimental tests.

The FEA models are available as completely automated software tools with user-friendly input interfaces, automated analyses, and postprocessing of results. The input interfaces allow the designer to select various package sizes, number and placement configuration of active elements, number and thickness of interconnect layers, via sizes, material combinations, and thermal and mechanical boundary conditions. The figure at the right shows the interface for input of geometry, material and boundary conditions for the global model. The results of the analysis are presented in the form of contour plots of stresses, temperatures, etc., at user- specified cross-sections.

Subsequent phases of the REL-TECH program will examine other technologies such as N-Chips' Silicon Circuit Board (SiCB) and Martin-Marietta's Chip-on-Board (COB). The CALCE EPRC is also soliciting requests to utilize this approach on other advanced packaging and interconnect technologies. For example, the Center is currently funded by Texas Instruments to apply their AIT modeling approach to TI Pyroelectric Uncoded Focal Plane Array Module (UFPA). For further information call Dr. Abhijit Dasgupta at (301) 405- 5251.

Plastic Encapsulation of Microelectronics

The CALCE EPRC in cooperation with Allied Signal, Boeing, Collins - Rockwell, Eldec, Honeywell, M/A Com, Navy - Crane, Sonix, Simmonds Precision, Westinghouse, and other member companies of the center, is developing a methodology to demonstrate reliability and to understand the limitations of plastic encapsulated microelectronics for storage, testing and usage profiles. The methodology will incorporate a set of procedures and guidelines that specify how to select, how and when to screen, how to qualify, how to handle, and how to manufacture plastic packages. The goal is to provide members with the science-based procedures, guidelines and process controls to realize the advantages of plastic packages in actual applications.

The program plan consists of seven tasks. The tasks are:

- Industry trend search
- Identify likely failure mechanisms, failure sites, and failure modes from acquired reliability and failure analysis data
- Develop physics-of-failure based models
- Analyze results of CALCE members reliability assessment tests for model validation
- Analyze results of CALCE members reliability
- Derive screening guidelines
- Derive qualification guidelines
- Derive guidelines for manufacture of plastic packages

Science-based reliability prediction models for the failure mechanisms are being identified and developed where necessary. Numerical techniques will supplement the development and application of the models. In some cases, the numerical analysis may provide insight to the development of closed-form models. This is especially important where interactions between different types of stresses and failure mechanisms complicate the closed-form modeling process. For example, a thermal stress cycle can trigger stress-assisted corrosion and stress-corrosion cracking. Furthermore, the determination of residual stress conditions and subsequent failure processes will aid in defining adequate test and screening methods.

The definition of what constitutes a "defect" will be rooted in the relevant failure mechanisms. Screens will address failures resulting from the identified failure mechanisms from the experimental tasks and best practices by industry. The modeling effort is designed so that screening and qualification guidelines can be derived directly. The crucial step is to determine the appropriate methods and/or intensity of "stress" required to precipitate the screening failure mechanism. The effect of screening on the measurement of plastic packages reliability will be examined using step stress and error-seeding techniques.

The documentation will present tailorable test methods to cost- effectively precipitate the same failure mechanisms which could have compromised long-term reliability in the field. Methods for overstress tests will be provided to qualify a product for potential overstress service loads and describe the impact of a manufacturing process on the overstress "strength" of a material and/or sub-assembly. Qualification documentation for wear-out failure mechanisms will be provided in terms of accelerated testing methods.

Boeing-DoD Qualification Studies for SMA

The Boeing Commercial Airplane Group and the Department of Defense have initiated a research program at the CALCE Electronic Packaging Research Center to develop methodologies for reliability enhancement using the results of highly accelerated stress exposures applied to the use environment. The philosophy behind this effort, called the Stress Margin Approach (SMA), focuses attention on design and manufacturing issues that are largely within the control of equipment manufacturers. The SMA replaces the current design guidance extracted from statistical reliability predictions dominated by electronic devices.

Assembly designs and processes, rather than individual devices, are now seen to be the important topics

that affect reliability of electronic boards and boxes, and they receive major attention within the SMA. The SMA uses as a central metric the exposure of electronic assemblies to highly accelerated stresses that force failures in weak or marginal areas. The stress exposures validate the designs, products, and processes, and provide confidence that products contain adequate stress margins above the stresses of the use environments.

The SMA relies at all stages on a continuing process of failure stimulation, root cause identification, corrective action, and retention of lessons learned. It recognizes that the process is iterative, and that the continuing construction of design models can reduce the number of validation failures. Highly accelerated stresses are employed at two major phases; for validation of product design and for process control monitoring. The process of product improvement using failure cause identification and corrective action continues for the life of the program. Service failures receive close attention, because a failure in service is an indication of deficiencies in the upstream design and manufacturing flow. The SMA philosophy audits and improves the upstream processes so that future production does not contain the potential for similar failures.

The emphasis in SMA is not to "fix it and ship it," but more importantly, fix the cause as well. In this approach, suppliers will be required to develop and describe their SMA implementation plans to customers. The schematic diagram below indicates the major elements of the SMA. To accommodate this initiative and expand laboratory capabilities, the following new equipment has been procured by the CALCE EPRC:

- Combined load chamber capable of simultaneous 6- axis random vibration and 70øC per minute rate of temperature change;
- High strain-rate MTS servo-hydraulic test frame;
- Three temperature-humidity load chambers.

In addition, existing failure diagnosis equipment will be used including:

- Infra-red microscope;
- Acoustic microscope;
- Environmental scanning electron microscope.

The test plans include simulation, testing and failure analysis of actual production hardware obtained from member companies and other sources. For further information, contact Dr. Abhijit Dasgupta at (301) 405-5251.

Connector Reliability Modeling

The reliability of electronic systems is largely dependent on and significantly affected by the performance of the various connectors in the systems. In close coordination with AMP Inc., a leading connector manufacturer, the CALCE EPRC is developing a physics-of-failure based mathematical model for determining connector reliability.

AMP has provided the EPRC with normal force-contact resistance data from Mixed Flowing Gas (MFG) tests conducted on phosphor-bronze specimens with a 50 æ" CoAu plating on a 50 æ" nickel underplate. The MFG test is an accelerated environmental test applied to study the effects of various environments on the corrosion of metals. The data consists of contact resistance as a function of load for various exposure times in the accelerated class II and III environments.

An estimate of the mean and standard deviation of the contact resistance to each of the normal forces was calculated for different aging periods in the two environments. A physics model based on the classical resistance law consisting of constriction and film resistance was used to develop and relate the

mean and standard deviation of resistance to normal force and aging. The Stennet, Ireland and Campbell model was used to model the stress relaxation in the connector socket springs over time and temperature.

The connector reliability model also incorporates environmental conditions in a mechano-stochastic manner. The model can be used to determine the probability of contact resistance occurring as a function of normal force, time, and temperature for different environmental aging classes.

Preliminary wear tests have been conducted to determine the relationship between the decrease in plating thickness and increase in the number of mating cycles. Also, improved wear tests are now in progress to study durability parameters. The CALCE Environmental Scanning Electron Microscope is being used to measure the decrease in plating thickness of the tested samples. On the completion of these tests, the effects of contact finishes durability on connectors performance will be incorporated into the model.

The model will be evaluated relative to force and contact radius using Hertz equations. An "end-of-life" criterion will be included in the model to enable it to predict the service life of the connector as a function of contact resistance. The CALCE connector database will be modified using available AMP databases and necessary test procedures will be outlined to provide the database with information for any connector. The model is being incorporated into the CALCE software.

Workshop on Temperature Effects

The first workshop on The Influence and Modeling of Temperature on Microelectronic Reliability was held at the CALCE EPRC on August 25, 1992. The workshop was attended by over one hundred people, including national and international experts. The workshop addressed the issue of higher reliability associated with lower temperature and the use of the Arrhenius relationship between temperature and reliability.

Various papers presented at the workshop addressed the relationship between reliability and temperature. Joseph Kopanski from National Institute of Standards and Technology (NIST) stated that, "the increase in reliability achievable through component power derating or improved equipment cooling is smaller than is often assumed. Furthermore, relatively little can be obtained by derating or cooling below a certain temperature range." Kopanski then outlined factors other than temperature which affect device reliability. The factors included electric field, current density, spatial temperature gradients, time rate of temperature change, thermal cycling magnitude, and initial defect density. Sorin Witzmann from BNR, Canada, confirmed this, noting that, "Static high temperature operation does not constitute a major factor in reducing the device life expectancy. Device life tests under static electro-thermal conditions for 10,000 hours at 170øC had shown survival rates higher than 99.9%. Cooling alone will produce an insignificant improvement for devices operated between their functional limits."

There was general agreement that solutions to device reliability lie in the identification of the degradation mechanisms and the factors controlling the degradation mechanisms. Sorin noted that, "Most of the device failures are related to design errors for new designs and defect-related failures for mature technologies. The defects included metal strip defects, metal interlevel connection defects, gate dielectric defects, polysilicon short defects, contact or interconnection step coverage defects, and contact Al/Si interdiffusion defects. Field return data has shown mechanical failure to be the most common incident with 70% of the failures concentrated in one or two devices, and 90% of the failures for a specific device related to the same failure mechanism." An example of defect-oriented device failure was given by Anthony Gallo from Dexter Corporation. Anthony talked about antimony contamination-actuated intermetallic formation at high temperature stress(= 200øC).

The non-randomness of device failures was presented by Dr. Stewart Peck who stated that, "Device failures are not random failures. Temperature affects the failure distribution and not the failure rate. Steady state temperature thus may not be the dominant accelerator when some crucial failure mechanisms actuated by temperature may not appear till beyond the expected life of the system."

The validity of using the Arrhenius equation to model the temperature dependence of device reliability was addressed by Joseph Kopanski as well as Mike Cushing from Army Materiel System Analysis Activity (AMSAA). Kopanski stated, "There is ample evidence that a straight-forward application of the Arrhenius equation with activation energies determined from high temperature accelerated stress testing is not strictly valid for predicting real device lifetime..." Michael Cushing stated that, "review of early literature demonstrated that the Arrhenius model at the device level was treated as a self- evident approximation based on the belief that most microelectronic failure mechanisms involved chemical or diffusion processes. Review of the basis of the Arrhenius for of the temperature-pi-factor in MIL-HDBK-217 revealed some fundamental study flaws. All the failure mechanisms had been lumped together without any root cause analysis... The implicit and fundamental assumption made in the study was that only steady state temperature was important, ignoring the effects of temperature cycle magnitude, temperature gradients, and time dependent temperature change."

Steve Martell from SONIX demonstrated the effects of temperature cycle magnitude and time-dependent temperature change on plastic package reliability. A majority of plastic package failures were attributed to T actuated wirebond failures, delamination at the chip-molding compound interface, chip-leadframe interface and molding compound-leadframe interface, and temperature transient actuated plastic package cracking, widely known as the "Popcorn" effect. Dr. Winterbottom from Ford Motor Company stated that "Reliance on temperature reduction as a means of reliability improvement is misleading, because some damage mechanisms operate at lower temperatures only." Examples of such mechanisms include hot carrier degradation in submicron technologies.

New Books

Reliability of Gallium Arsenide MMICs, edited by Dr. Aris Christou, published by John Wiley.

Placement and Routing of Electronic Modules, edited by Dr. Michael Pecht, published by Marcel Dekker, Inc.

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CALCE News

May 1993

Plastic Package Reliability Study

The use of non-military microcircuits offers advantages of cost, size, weight, and availability. The traditional barrier to their use has been perceptions of lower reliability in military, space and commercial aerospace applications. However, the avionic and military electronic industries have begun to reconsider the use of plastics due to (1) improvements in reliability of non-military microcircuits; (2) a heightened level of skepticism about the traditional probabilistic reliability prediction methods used in industry; (3) improved methods of accelerated testing and deterministic reliability predictions; (4) awareness that factors other than "part reliability" are more important than previously thought; (5) concerns that some military part numbers may not be available throughout the life of commercial aircraft under development; and (6) relentless cost pressures that can be eased by the use of commercial parts.

Under a cooperative agreement with Eldec Inc. and the CALCE EPRC members, accelerated testing is being conducted under a variety of stress conditions. Using appropriate acceleration models and failure distribution parameters, the reliability of the products under use conditions are being estimated. The parts being tested are plastic encapsulated modules representative of four general families of microcircuits.

Sixteen hundred samples, representing three different part numbers from four different suppliers, were assembled on circuit cards and tested in accelerated environments. Each sample was exposed to a combination of temperature cycling, temperature-humidity-bias, and vibration, as defined by a Taguchi orthogonal array of stress factors. Of special note in this work are the following:

- The parts were tested after being assembled onto printed circuit cards using representative soldering processes, as contrasted with the 'typical' approach of testing unassembled parts.
- Test data included parametric data as well as pass-fail data.
- Parts were tested at various points throughout the environmental conditioning, not just at the beginning and the end.
- A mix of environmental stress conditions was applied to each test sample according to a Taguchi array, in order to allow evaluation of possible interactions among stress conditions.

Three separate accelerated environmental test conditions were used: temperature cycling, temperature-humidity-bias (THB), and vibration. The three environmental conditions were arranged in an L16 Taguchi array, and the 16 racks of CCA's were assigned accordingly. Temperature cycling was evaluated at four levels, as shown in Table 1.

Table 1. Levels of temperature cycling

Table 1. Levels of temperature cycling

Level	Temperature Range	Mean Temperature	Temperature difference
1	-55 to +125 C	35 C	180 C
2	+50 to +125 C	85 C	75 C
3	0 to +75 C	38 C	75 C
4	+75 to +150 C	113 C	75 C

THB was evaluated at two levels, an 85% RH-85øC with operating bias, and room ambient with no bias. To avoid drying of the samples due to localized heating, the operating bias was switched on and off at half-hour intervals. Two levels of vibration testing were evaluated. Level 1 used random vibration and level 2 was no vibration.

Using this array, a unique combination of environmental treatments was assigned to each rack of CCA's. The conditions were applied sequentially, with test points at half decades of either temperature cycles or hours of THB. Vibration was introduced only at the beginning, the middle, and the end of the test flow.

After testing through 2,000 temperature cycles, 2,000 hours of temperature-humidity-bias, and vibration, two types of results were obtained from this experiment: pass-fail, and electrical parameter shifts. Some failures occur by accumulated damage, in which a given parameter shifts over time, with the magnitude of the shift increasing with duration under stress until the part fails. Other failures show no evidence of degradation until failure occurs.

For the conditions tested, the preliminary results indicate that plastic parts can be used in avionics environments. However, there are reliability differences among part manufacturers and part numbers. In addition to these tests on small logic devices, tests are also being conducted on three other part families: small signal transistors and diodes, power semiconductors, and large logic and memory devices. Some of those tests are already complete, and data will be available from all of them by the end of August.

Materials Database Available

The CALCE EPRC is in the final stages of establishing a center for electronic material testing, characterization, and computer database access in consultation with its members and the government. The goal is to provide a national resource of high quality and very affordable information on electronic materials by:

- cataloging the materials used in electronics, including conventional and new composite materials;
- characterizing material properties, including coefficient of thermal expansion, dielectric constant, thermal conductivity, shrinkage, specific heat, thermal and electric conductivity, density, modulus of elasticity, fracture strength, porosity, homogeneity, plate-ability, machinability, solder/weldability, and other parameters required to establish the electric, thermal, mechanical, corrosion, optical, and stress interaction behavior;
- using design of experiments to determine any interactions of material parameters due to operating or environmental conditions, including frequency, temperature, moisture, altitude, and processing conditions;
- establishing standard models and test conditions required to fully characterize the electronic packaging materials;
- enhancing the existing CALCE material database to conform to the ISO 10303 - Standard for Exchange of Product Model Data (STEP); this will provide a neutral format for data exchange and will enable the CALCE EPRC to provide the database and data models in an easily accessible

format that can be effectively used on a variety of CAD systems;

- using the CALCE EPRC's past experience, expertise, and unique position to coordinate information sharing with interested companies, universities, and government agencies.

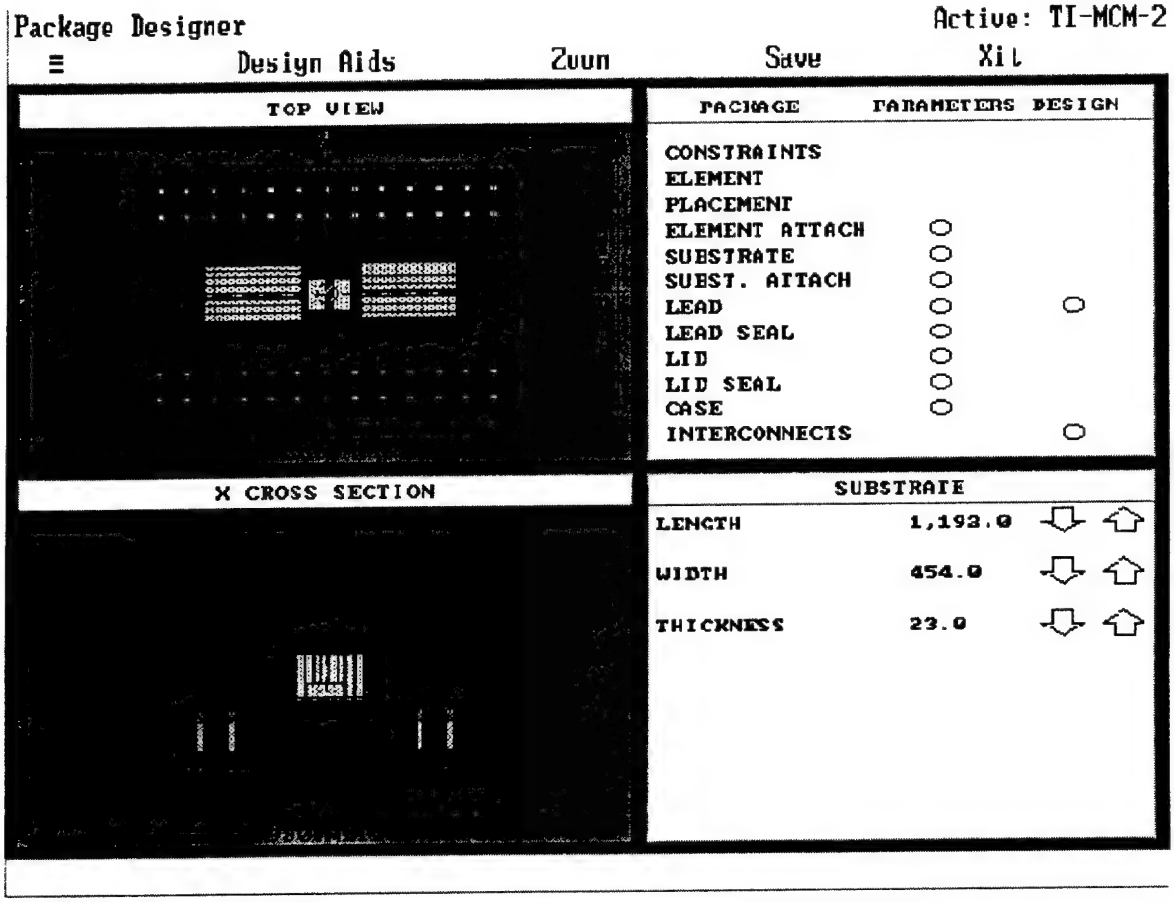
The proposed material database effort will change the way industry, government, and academia do business by providing access to an ISO compatible database. Our intent is to make the database available to all companies, with special support for those companies that provide test samples or test data. To be part of this effort, contact Dr. Pat McCluskey at (301) 405-0047.

Beta Version of POF Software Released

The beta phase coordination meeting for the Army sponsored Physics-of-Failure Reliability program was recently held to demonstrate the beta version of the microelectronic reliability assessment software, called CADMP, and to solicit help from the electronics community in the form of beta sites for software evaluation. The meeting was attended by representatives from industry, university, and government organizations. Thirty-six organizations have asked to become beta sites. The beta software implements many of the enhancements suggested by alpha sites.

Reliability assessment of microelectronics has traditionally been based on failure rate equations derived from field-failure data, where the actual failure mechanisms of the product were not identified. These failure rates have served as inputs to other design and testing tasks, which have been therefore, misguided. On the other hand, the physics-of-failure approach utilizes the scientific knowledge of failure mechanisms to prevent product failures. Product reliability is assessed using failure models that relate the stresses due to environmental conditions, product geometry, and materials at potential failure sites.

CADMP consists of design and analysis utilities supported by reusable libraries. The mission and test profile utility, in conjunction with the environment library and the tests and screens library, defines the mission loads and durations. The design utility enables package geometry design and selection of package materials from the materials library. A reliability utility uses the models from the failure mechanism library to provide the time-to-failure for potential failure mechanisms at potential package failure sites. For more information, contact Dr. Pat McCluskey at (301) 405-0047.



3D die stack module in CADMP.

Statistical Distribution Software Available

Parameters for life distributions are typically determined by plotting failure time data by hand on probability paper. The new CALCE Statistical Distribution Software simulates this process for Weibull, Normal and Log-Normal distributions by utilizing Johnson's theory of order statistics with ranking, which provides percent failure estimates. Cumulative failure probability (percent failure) versus time-to-failure data can be plotted to determine the underlying distribution. The distribution that produces the best fit straight line of percent failure versus time to failure on the appropriate logarithmic scales is the estimate of the underlying distribution for the data. The best fit is determined by linear reduction analysis of each distribution.

Each of the Weibull, Normal and Log-Normal distributions can be described by three functional relationships: cumulative failure probability, failure probability density, and failure rate distributions. Each type of distribution can be graphed to illustrate distribution shapes. The software which helps experimental data analysis and assessment, comes with a documentation; a support line is also available. The cost of the software is $90. For more information, contact Joan Lee at (301) 504-5323.

Design for Environmental Compatibility

Most designs currently do not account for environmental compatibility of the finished product, in terms of waste management and materials recovery. The CALCE EPRC is currently addressing design for environmental compatibility with emphasis on recycling manufacturing scrap products and finished products at the end of useful life. Product recovery typically occurs in three major forms: (a) repair and reuse of scrap products from the manufacturing line, or from the customer at the end of useful life; (b) material recycling; or (c) reuse of parts and re-manufacture. Some of the issues addressed in the design

for environmental compatibility include the following:

- Design for disassembly: Product parts must be separable to allow easy disassembly before disposal for material recycling, or to allow disassembly for recovery of reusable components.
- Material selection and identifiers - design for recycling: Material recycling is typically accomplished by shredding the material and separating it into component parts by special techniques. Most manufacturers label their recyclable parts with material identifiers that give the composition of the part to allow easy identification. Materials that can be recycled easily are also identified early in the design process, and the number of materials used in design is minimized.
- Degradability and wastefulness: The degradability and wastefulness of the materials used is evaluated early in the design phase. The evaluations are translated into design recommendations to aid material selection.
- Economics of environmental compatibility: Material recycling involves trade-offs between the value that can be recovered and the amount of effort made to collect, separate, and recover the parts and materials. Reuse and re-manufacture also involves trade-offs between product value and the time involved in disassembly, inspection, cleaning, testing, replacement, repair, and reassembly.

The CALCE EPRC is currently addressing computer tools for automating product evaluation for environmental compatibility. These include the following:

- automated material selection and substitution for environmental compatibility;
- automated disassembly analysis and repair, involving optimization of disassembly versus recycling decisions, considerations of compatible and incompatible materials, and costing of the disassembly process.

For further information on this project, contact Mike Pecht at (301) 405-5323.

Vibration Assessment of Wedge Locks

To calculate the fatigue life of components mounted on a printed wiring board (PWB), an estimate of the PWB natural frequency is required. One of the most dominant parameters that influence the boards natural frequency is boundary conditions. A series of experiments were conducted with Calmark three-part and five-part wedge locks to determine boundary condition restraints. The rotational spring constant for the wedge lock was calculated by measuring the natural frequency of the plate. The wedge locks were then modeled for use in the CALCE software.

For sinusoidal accelerations between two and fifteen G's, the wedge locks were found to behave as constant linear elastic rotational springs. For higher accelerations and larger edge rotations, the wedge locks behave with a non-linear, softening, spring constant. The wedge lock restraint was found to be approximately directly proportional to the tightening torque.

The five-part wedge lock provided more rotational restraint than the three-part wedge lock. For the manufacturer's recommended torque of 6 in-lb, the non-dimensional rotational spring constant for the three-part wedge lock was found to be about 2, while for the five-part wedge lock it was found to be about 5. The wedge locks were found to provide an approximately constant boundary condition fixity, in contrast to Steinberg's results (1988). The wedge lock performance was also found to be relatively insensitive to small variations in mounting slot thickness. Contact Don Barker at (301) 405- 5264 for more information.

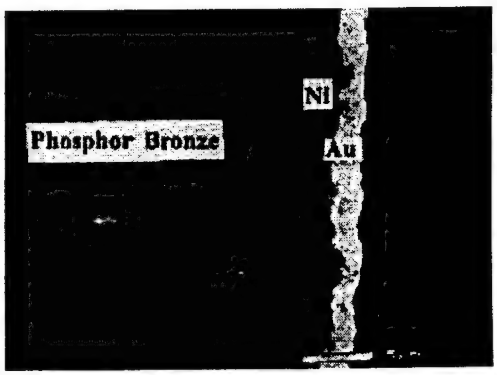
Reliability of Electronic Boxes

The Defense Modeling and Simulation Office of the DoD has recently funded a collaborative research effort between the Army, the CALCE EPRC, and the University of Iowa Center for Simulation and Design Optimization (SDO). This $.5M research program will exploit and link the ongoing modeling and simulation research programs from these institutions. Currently missing in electronic system reliability analysis and prediction is computer simulation, from the circuit card level upward in the electronic system. This project is directed at providing such a link for powerful, proactive evaluation of electronic systems.

SDO will be responsible for tools that will provide dynamic load information at the electronic box level from platform levels, such as a vehicle. The CALCE EPRC will produce software simulation tools to interface the external environment of the electronic box to existing CALCE circuit card and component level reliability simulation tools. For further information on the project, contact Don Barker (301) 405-5264.

Wear Testing of Connectors

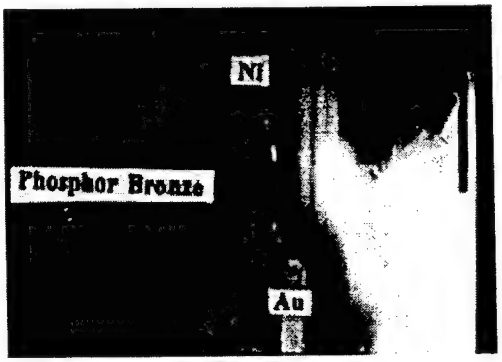
The CALCE EPRC is continuing the AMP Inc. sponsored connector reliability modeling effort by enhancing the "first- cut" model developed during 1992. In developing a "first-cut" model, CALCE performed data analysis on mixed flowing gas (MFG) contact resistance versus normal force data, and used statistical tools to model the contact resistance as a function of the connector materials, the usage environment, time in the usage environment, and stress relaxation in the contact springs. A contact-physics model based on the classical Holm's equation was used to develop and relate the experimental contact resistance data to normal force and aging.



The model also accounts for wear in the contact finishes as a function of the number of cycles to expose the underplate. Data obtained from wear tests conducted on plated metallic coupons was used in modeling wear. In order to obtain a better estimate of the wear, wear tests are now being conducted on actual connector samples.

A wear testing fixture has been developed which enables the hand mating-unmating of connectors and simulates actual field conditions. An Instron machine is unsuitable for cycling purposes, as it induce wear that is uncharacteristic of field conditions.

Connector pins and springs were extracted after each stage of cycling and were cross sectioned at the wear tracks. The cross sectioned specimens were observed under the CALCE Environmental Scanning Electron Microscope (ESEM) to determine the reduction in gold plating thickness with cycling.

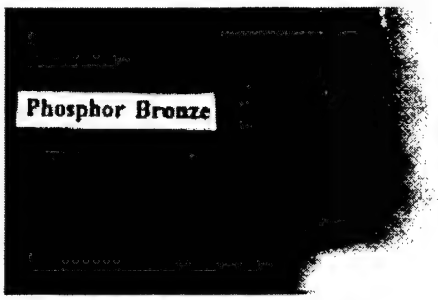


The top picture shows the gold plating and the nickel underplate on the pin initially. The next picture down shows the pin after 600 mating-unmating cycles. A wear track is visible in this picture where the gold has worn away. The picture just below shows the pin after 1,000 cycles; the gold plating is non-existent in this picture.

Tests are now being conducted to determine the variation in plating thickness along the length of the wear track, by cross sectioning the pins at various stages along the length of the track. These data will be used in conjunction with data from MFG tests conducted on coupons of varying plating thicknesses to

reinforce the wear model.

The CALCE EPRC software program for connector reliability is in development and an alpha version will be available in October. For more information, contact Rod Martin at (301) 405-5325.



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CALCE News

September 1993

Combined Vibration and Thermal Loading

A QualMark (Denver, CO) OmniAxialTM Vibration System combined with an UltraRateTM Thermal System has recently been installed as part of the CALCE Electronic Packaging Research Center experimental facilities. The single chamber that houses the two systems provides simultaneous vibration and thermal loading and is intended for use in the Stress Margin Analysis (SMA) project.

The vibration system provides random outputs along six degrees of freedom (three translations and three rotations), at a maximum of 90 GRMS over a bandwidth of 0-2000 Hz, and at a maximum force of 2,400 lbf. The noise rating is less than 65 dba. The thermal system has a temperature range of -77 to 200øC, with a ramp rate of 60øC/minute using a 20-lb aluminum load. The work space is 15"w 17"d 15"h, with a 12" square mounting table and a 4" diameter port for external access. Possible experiments include thermal, vibration, or combined thermal and vibration. The chamber temperature ramp rates are fast enough for most thermal shock experiments.

This equipment is currently being used to develop guidelines for the Stress Margin Approach to reliable electronics. The underlying concept in this approach is to compare the ruggedness (resistance to overstress failures under highly accelerated loads) of new products with those of existing successfully operating products.

If the failure mechanisms and stresses at the failure site are similar for both the new test article and the existing comparison article, then it can be argued that new products that last longer than the comparison article under highly accelerated test loads (that is, have a higher "stress margin") will exhibit higher reliability in the field. The aim of the test is to provide comparative reliability data relative to an expected benchmark, rather than an absolute reliability or life prediction.

The QualMark system is currently being used to experimentally evaluate the Stress Margin Approach on several different test articles. In addition, industry-provided samples of printed wiring boards, SIMs (Serial Interface Modules), and R-F couplers are scheduled for tests at the CALCE EPRC facilities later this year.

For information about the CALCE EPRC use of this equipment or about the Stress Margin Approach, please call Dr. Abhijit Dasgupta at (301) 405-5251. For information about QualMark equipment and testing capabilities, please call Preston Wilson at (303) 254-8800.

Highly Accelerated Stress Tests

Highly Accelerated Stress Test (HAST) chambers from ESPEC Corporation (Grand Rapids, MI) have recently been added to the growing CALCE EPRC list of experimental facilities. These chambers have an unsaturated control system that leaves no condensate on specimens. A wet and dry bulb temperature control system helps precisely control environments before, during, and after the tests. An internal fan reduces gradients common to dual-vessel HAST chambers.

The HAST chambers are currently being used to conduct tests on printed wiring boards as part of a reliability program to establish guidelines for the design PWBs that are resistant to conductive filament formation. Conductive filament growth is the loss of insulation resistance in organic laminates between

conductors due to dendritic growth under accelerated conditions of temperature and humidity.

Plastic-packaged integrated circuits are also being tested in the HAST chambers for moisture absorption, one of the major reliability concerns in such plastic packages. The tests are conducted at constant temperature and humidity, with the percentage moisture gain monitored to identify the equilibrium moisture content.

Tensile Tests of Polyimide Films in E-SEM

Tensile tests to investigate the microstructural and mecanical properties of polyimide films are being performed in an Environmental Scanning Electronic Microscope (E-SEM). Films, such as Kapton and Ultem, are highly desirable in electronic packages due to their low dielectric constants, high thermal stability, and ease of processing. However, the control of mechanical properties is still under debate and microstructural control in film-manufacturing is a critical issue.

Research focuses on the tensile failure mechanisms of polyimide films, more specifically, on the morphological response to deformation and fracture. The changes during testing are recorded, and include crazing, yielding, and fracture data in situ. Results indicate that Kapton is sensitive to surface manufacturing defects and contamination--under tensile loading, crazes induced around the local defected or contaminated area propagate to flaws and eventually cause fracture. On the other hand, Ultem is not sensitive to surface defects or contaminations, as complementary experiments, polarizing transmission microscopy and Ar ion-bombardment technique are utilized before and after tensile test. The results also reveal the semi-microstructural (droplet) and microstructural (spherulite) morphology changes. For more information, contact Dr. Michael Pecht at (301) 405-5323.

Radiation Effects Facilities

Radiation effects capabilities have recently been added to the CALCE EPRC laboratory facilities through cooperative arrangements with the Materials and Nuclear Engineering Department. Radiation in electronic packaging has always been critical reliability issue since the discovery of the single- event upset, which was directly traced to cosmic-ray-induced nuclear reactions in the packages high atomic number materials. Until recently, commercial electronics have been immune to radiation hardening requirements. Radiation effects in commercial electronics have become more critical due to dual-use electronics and the necessity to use plastic packages in avionics.

A series of experiments on low-dose rate effects in plastic packages has been started in the facilities, which include a 25,000 Ci cobalt-60 source; a 2-9 MeV electron linear accelerator with separate target lines and environmental chambers; a UV/VIS and FTIR spectrophotometer and an ESR spectrometer. The facility is equipped to characterize structural changes that occur in plastic and polymeric materials. The electron linear accelerator, in combination with a specially designed atmospheric test chamber, is a unique national resource for the evaluation of radiation effects on electronics. For further information, contact Dr. Pat McCluskey at (301) 405- 0047.

A New Model for Solder Joint Fatigue

Existing solder fatigue models, based on a single loading parameter such as the cyclic strain-range or the total cyclic energy, assume that a single damage mode (creep, in this case) dominates the failure mechanism. This is unrealistic at low- temperature and high-frequency thermal cycles (as in accelerated testing and environmental stress screens), and leads to excessive conservatism. In reality, microstructural damage caused by elastic, plastic, and creep deformations are different and their relative magnitudes must be assessed separately, depending on the loading history.

The CALCE EPRC has developed an improved simulation, based on an energy partitioning approach,

that considers the complete stress-strain hysteresis response of the solder. The energy stored and dissipated during each cycle (determined by the hysteresis curve) is partitioned into elastic (recoverable) energy, plastic (instantaneous, irrecoverable) work and creep (time-dependent, irrecoverable) work. This energy partitioning information can be obtained easily from any viscoplastic analysis such as finite element methods. Three independent power-law expressions relating the partitioned energy to the damage (or cycles to failure) are obtained from experimental data in the literature for eutectic Pb-Sn solder. The total damage incurred in each thermal cycle is calculated from simple linear superposition of damage due to each of the three partitioned energy terms.

This method is generic to all viscoplastic materials and accounts explicitly for all loading histories including vibrational loads. This approach has also been used to simulate solder crack initiation and propagation, using damage mechanics concepts. Details of the approach are given in the following publications:

Solder Creep-Fatigue Analysis by an Energy-Partitioning Approach, A. Dasgupta, C. Oyan, D. Barker, M. Pecht, **ASME Journal of Electronic Packaging,** Vol 114, No. 2, June 1992, pp 152-160.

Numerical Study of Fatigue Life of J-Leaded Solder Joints Using Energy-Partitioning, S. Verma, A. Dasgupta, and D. Barker, to appear in **ASME Journal of Electronic Packaging,** 1993.

Solder Joint Crack Initiation and Crack Propagation in a TSOP Using Strain Energy Partitioning, D. Barker, V. Gupta, K. Cluff, submitted to **International Electronics Packaging Conference,** Sept. 1993.

For information on the TSOP (thin small-outline package) failure modeling effort, please contact Dr. Don Barker at (301) 405-5264. For information on the energy-partitioning model for creep-fatigue damage in solder, please contact Dr. Abhijit Dasgupta at (301) 405-5251.

TSOP Solder Joint Fatigue Failure

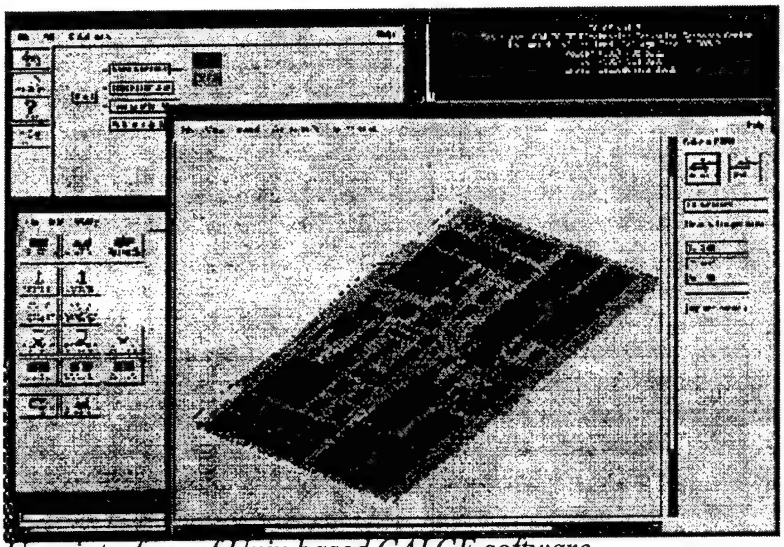
Unix Software Released

A Unix-based version of the CALCE software was recently released, marking the first venture into a networked graphical user interface (GUI) environment and providing a model for future software development. The hardware and software requirements for executing this new version are:

- Sun SparcStation with color monitor
- SunOS 4.1x
- 32 MB or more RAM
- 80 MB available hard disk space
- SCSI 1/4 inch cassette drive for installation
- X Windows versions X11R4 or later
- OSF Motif runtime version

This new version of the software provides the same core functionality embedded in the DOS version.

Lockheed - Fort Worth, a primary supporter of the Unix development effort, has praised the new Unix-based release. Bruce Bordelon of Lockheed comments that this software is more intuitive and it logically leads the user through the design and analysis of a printed circuit board model. For more information, please contact Dr. Michael Osterman or Tom Riddle at (301) 405-8023.



User interface of Unix based CALCE software

Physics of Failure for Microelectronics

The physics-of-failure effort sponsored by the U.S. Army, which included the development of the prototype Computer Aided Design of Electronic Packages (CADMP) software, was completed in July 1993. However, the CALCE EPRC has decided to continue to evolve the software independently. The second generation software, that will result from these efforts, is called CADMP-2 and incorporates the recommendations and suggestions received from industry and government organizations acting as beta sites. Highlights of the various changes and additions include:

Interconnect library - Design and selection of interconnect technology, standard technologies such as wirebond, TAB, Flip-TAB, Flip-chip, and HDI are included;

Parameter manipulation - Numerical values of failure mechanism library parameters may be modified by the user and then reprocessed to optimize the design;

Derating tool - Achieving desired life involves examining the dominant failure mechanisms. By varying the operating point on the derating curve, different stress combinations which would result in desired life can be identified;

Glossary - Attribute definitions were documented;

Report manager - Reports are generated on design, reliability assessment, testing, screening, and derating.

The new CADMP-2 software will be explained and demonstrated at the physics-of-failure meeting announced on page one of this newsletter. For more information, please contact Dr. Pat McCluskey at (301) 405-0047.

Optoelectronic Research Center

A new Optoelectronic Interconnects and Packaging (OEIP) Research Center was recently initiated at the University of Maryland. This is a joint industry/university cooperative research center (I/UCRC) sponsored by the National Science Foundation. Current industrial sponsors include AT&T, Texas Instruments, The National Security Agency, The U.S. Army, COMSAT, and AMP. The CALCE EPRC is directly involved with the research activities of the OEIP Research Center through the efforts of Dr. Aris Christou.

The OEIP Research Center goals are to develop and advance technologies for optoelectronic device integration and packaging; to impact low-cost, high-performance optical communication and data links; to improve manufacturability and reliability of optoelectronic components and subsystems; to explore new technologies applicable to displays, optical memories, printing, and sensors; and to investigate non-intrusive optical testing and diagnostics optoelectronic circuits. The research activities include the following:

Hybridized Receiver Array Chip - Development of a low-cost technology to interface a multi-channel waveguide array with a multi-channel receiver chip. In one approach, an array of single-mode glass waveguides on an optical interconnect chip is coupled to an array of silicon pin detectors on a silicon chip via a 45o mirror etched in the waveguide. The waveguide chip is flip-chip bonded to the silicon chip. In another approach, an array of single-mode glass waveguides, or a fiber ribbon, butt- coupled to a III-V pin waveguide photodetector array. The photodetector array is then flip-chip bonded to a silicon receiver array.

Free-space Optical Interconnects - Development of key optical elements for free space optical interconnects. The initial aim will be to produce diffractive optical elements (DOEs) with functions such as asymmetrical beam deviation or beam splitting for multiple fan-out. The DOEs to be realized will be the key components of the chip area-to-area and edge chip-to- area free-space interconnects. This activity will also develop the transmitter and receiver components to be directly connected to the nodes on the silicon circuits.

Manufacturing, Reliability, and Performance Simulation - Simulation of the figure of merit for free-space optical interconnects, waveguide optical interconnects, and holographic interconnects, taking into account the driver elements, the interconnect media, and the receiver element. The performance parameters for the figure of merit simulation include propagation delay, cross talk, and signal attenuation and will factor in temperature, reliability, and manufacturing tolerances and alignment.

Monolithic and Hybrid-integrated Waveguide Laser Devices - Design and fabrication of monolithic and hybrid-integrated waveguide laser devices to relax the tolerance of laser-fiber coupling and simplify the packaging of optoelectronics. This involves developing and refining key technology areas: micro-machining optical components and alignment keys; designing and processing monolithic or hybrid beam-expanding waveguide structures; and simple, precise packaging of optoelectronic chip-to-fiber and planar waveguides.

Process and Device Characterization - Development of non- destructive tests to evaluate the processing and packaging of devices from base substrate material, epitaxy, etching, and other stages in device fabrication, integration, bonding, and final packaging. Fiber and free-space optical probes have already been developed for mapping material temperature, doping density, defects, surface profiles, general high- resolution imaging, optical anisotropy resulting from processing defects, and ultra-high-speed characterization of devices at various stages of processing and packaging. The optical techniques include, scanning surface slope profiling with single-atom high-step resolution, fiber-based scanning confocal microscopy, picosecond electro-optical sampling, optical measurement of S parameters in MMICs and high-speed OEICs, birefringent imaging of surface anisotropy (particularly in InGaAsP-based structures), and ultra-high- resolution microscopy of fine-line (100nm) lithography.

Hybridized Optical Transmitter Array Chip - Development of a low cost approach to implementing an optical transmitter array, using standard silicon (GaAs) driving circuitry and a single-mode dielectric waveguide integrated laser array. The optical transmitter system consists of a flip-chip-bonded laser

array and a waveguide directly coupled to a receiver chip to realize a hybrid chip-to-chip optical interconnect.

Waveguide Waferboard - Development of technology for fabricating low-loss single-mode glass or polymer waveguide optical interconnects. In the future, this technology can be expanded to implement star couplers, Y-branches, beam splitters, and beam-steering optics.

The OEIP Research Center aims to integrate functional optical and electrical devices using 3-D growth techniques, 3-D etching, flip-chip bonding, V-grooves, and silica-polymer waveguides. Using the fabrication facilities at the University of Maryland, optical components such as ball lenses, lenslet arrays, CAIBE/RIE etched mirrors, integrated beam splitters and gratings will be used to demonstrate and implement optical interconnect systems. For more information concerning the OEIP Research Center, please contact Dr. Pat McCluskey at (310) 405-0047.

New Soldering Book

Soldering Processes and Equipment, edited by Dr. Michael Pecht, published by John Wiley & Sons, New York, 1993.

Created: 5/21/95 Updated: 11/10/95

CALCE News

February 1994

Electronic Packaging of Power Supplies

Companies capable of building smaller, more reliable, and more cost-efficient power supplies will have a substantial competitive advantage in the global marketplace. Establishing this advantage requires creative and scientifically evaluated electronic packaging. Toward this end, the CALCE EPRC is working jointly with LZR Electronics, a small Maryland company specializing in the design and manufacture of the miniature switching power supplies typically used in notebook, lap-top, and hand-held computers, as well as in other electronic peripherals and instruments.

The intent of the multi-phase research project is to draw on the expertise of the CALCE EPRC to provide LZR Electronics with methods and software for improving packaging designs. Under a Maryland Industrial Partnerships (MIPS) grant from the State of Maryland, administered by the Engineering Research Center, Phase I has been successfully completed and Phase II has recently begun.

During Phase I, creepage and clearance requirements for printed wiring boards (PWBs) were characterized as functions of voltage and insulation type. Prototype routing software was developed, incorporating various electrical guidelines.

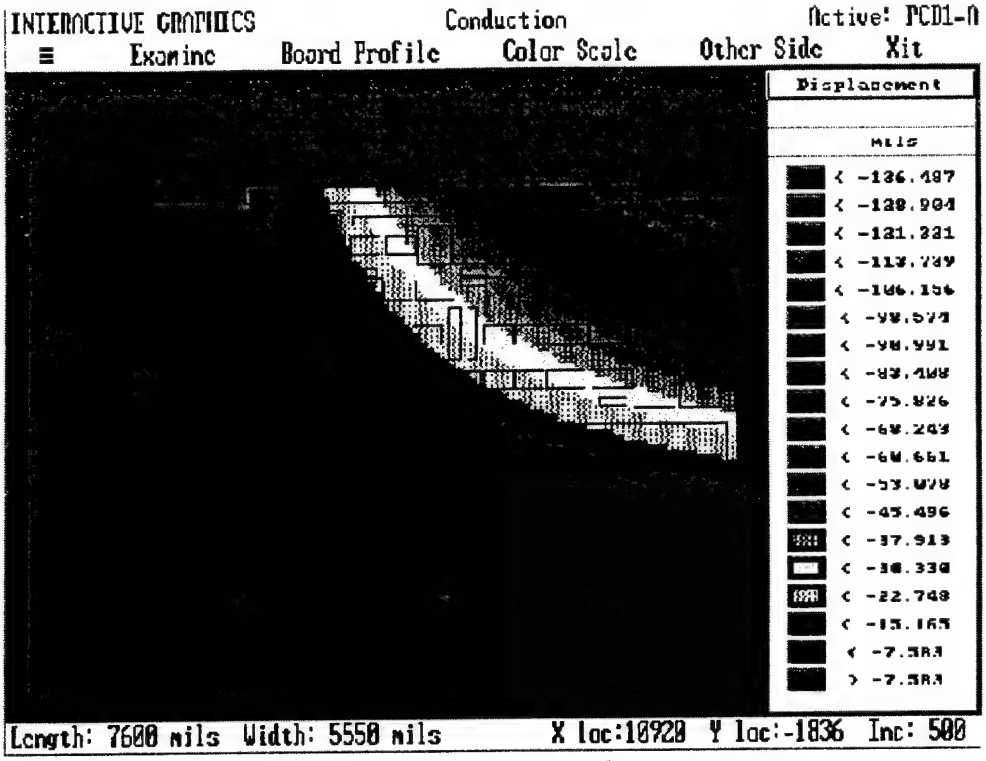
During Phase II, enhancements will be made in the PWB routing software to incorporate additional electrical guidelines, including the clearance between metallization tracks as a function of the voltage differential between tracks for a given insulation. Capabilities for estimating temperatures at the system level will also be developed. Thermal and vibration tests are planned on prototypes to experimentally validate reliability. For more information, please contact Dr. Yogi Joshi at (301) 405-5428.

In-plane Motion Under Vibration Loading

A new program module is being developed in the CALCE Software for printed wiring board (PWB) analysis to calculate the in-plane motion of a PWB subjected to vibration loads. The program will calculate the in-plane component of out-of- plane PWB vibration. The long-range goal of the project is to assess wear in the edge card connectors resulting from in-plane PWB motion.

The figure below is an example of the graphical output from the new software. This figure is a contour map of in- plane displacements corresponding to the first fundamental out- of-plane vibration mode for a PWB supported along the left edge with a single support point at the lower right corner. The figure has been generated from an algorithm that uses the out-of-plane mode shape data generated by a finite element vibration tool, and does not require a more complicated non- linear geometric analysis. Currently an improved version of the original algorithm is being subjected to a series of verification tests.

The new addition to the CALCE PWB software will require the user to specify in-plane boundary conditions. Initially, the only boundary conditions will be fixed or free; in-plane frictional forces, such as those that would occur with a real edge-card connector, will be added later. The final goal is to incorporate a wear model to assess connector life based on a plating wear model. Contact Dr. Don Barker at (301) 405-5264 for further information on the project.



Graphical display of PWB in-plane motion analysis.

Derating Project Sponsored by SRC

The CALCE Electronic Packaging Research Center has been awarded a contract by the Semiconductor Research Corporation (SRC) to develop derating software tools addressing the reliability of microelectronic packages. Derating is a technique through which stress levels on a component are reduced as a means to enhance reliability. Typical derating parameters include junction temperature, voltage, current, and frequency, depending on the device type.

Typically, guidelines for thermal derating involve reduction of junction temperature, based on the belief that device reliability is an Arrhenius function of steady state temperature. However, current studies by the National Institute of Standards and Technology (NIST) and the CALCE EPRC have questioned the rationale of using the Arrhenius relationship and the concept of device activation energy to calculate temperature acceleration of device failure rate.

Some of the questions include: Will a lower temperature improve reliability? If there is a need to lower temperature, what is the value of the lower temperature? Does the maximum operating temperature vary with microelectronic package design? Is it possible to change a parameter other than temperature to achieve the designed mission life and to escape the penalty of added cost and weight associated with cooling methods?

The goal of this project is to develop derating methods and software that can be integrated into existing modeling/design frameworks. The initial focus will be on derating junction temperature. The software capabilities will include:

- derating approach to assess variabilities in material properties, geometries and application environments;
- acceleration transforms correlating rated to derated conditions; and

- multi-variable analysis methods to evaluate the combined effects of various geometries, materials, and application environments on derating.

The derating software will be used to assess microelectronic packages, based on a set of fundamental inputs for geometry and material properties. For more information, please contact Dr. Pat McCluskey at (301) 405-0047.

Reliability of Electronics at the Box-level

Currently missing in electronic system reliability assessment is computer modeling and simulation from the circuit card level upward in the electronic system. The CALCE EPRC's PWB-level software has been available for over five years, and the new component-level software (Computer-Aided Design of Microelectronic Packages, or CADMP) is being beta-tested by over fifty government and industrial members. To proactively assess the reliability of electronic systems at the box-level, a new and complementary set of software tools is being developed under a $500K research project funded by the Department of Defense Modeling and Simulation Office (DMSO). This project is a collaborative effort between the U.S. Army, the CALCE EPRC, and the University of Iowa Center for Simulation and Design Optimization (SDO).

The modeling and simulation objectives of the new project are divided into three tasks: the calculation of the dynamic loads at the location of an electronic box; the calculation of loads transmitted through the box to the PWBs; and the reliability assessment of the electronic box itself. Iowa SDO will calculate the dynamic loads and motion history surrounding the electronic box, while the CALCE EPRC will concentrate on transferring the load information to the PWB level and developing the new analysis capability to assess the reliability of the box.

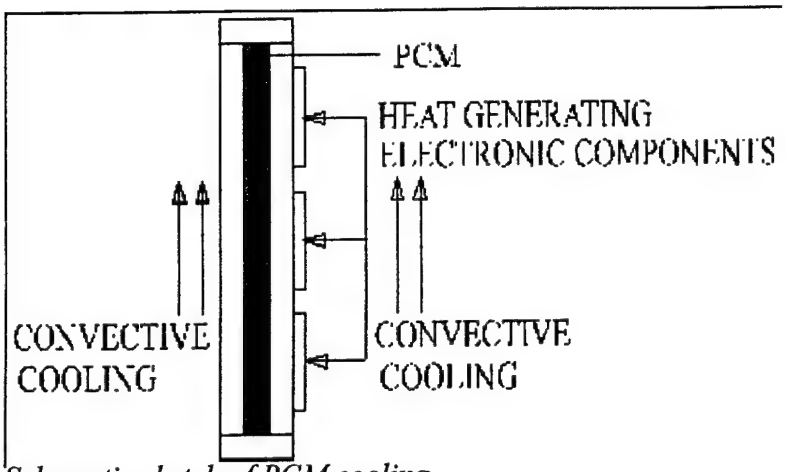
As an example test case for this project, the Iowa SDO is performing a dynamic simulation analysis of a High Mobility Multi-purpose Wheeled Vehicle (HMMWV), a multi-use Army combat vehicle, as it is traversing a prescribed terrain. The dynamic load and motion data at the location of two preselected electronic boxes will be transferred to the new box- level reliability assessment software. Additional environmental loads, including temperature, humidity, chemical contamination, and radiation, will be specified by the user.

The CALCE EPRC is currently assembling a library of generic, representative box-level failure mechanisms. These-- and associated physics-of-failure box-level models--will be parsimonious models that employ the fewest possible parameters to assess accurate time and cycles to failure. These parameters will help identify key characteristics that need to be controlled during design and manufacturing to maximize design durability.

The project goal for the first year is to provide an alpha version of the box-level software to get alpha-site support from industry. A second-year effort is planned to improve the robustness of the software and to increase the sophistication of the load transfer and failure models. For further information, please contact Dr. Don Barker at (301) 405-5264.

Phase Change Materials

For a number of years, phase change materials (PCMs) have been used for solar energy storage and space applications involving pulsed power loads. Such materials have a large latent heat, allowing absorption of large thermal loads during transient periods without significant temperature change. The thermal energy can be released to the environment over an extended period of time.



Schematic sketch of PCM cooling

The use of PCMs for electronic cooling appears to be a promising application. Therefore, the CALCE EPRC, with support from McDonnell Douglas Aerospace and Texas Instruments, is examining the applicability of PCMs for thermal control during transients. An analytical and computational study, focusing on three-dimensional transient analysis of an electronic circuit module cooled by PCMs, is being conducted during the first phase of this research. The analysis examines coupled heat conduction, as well as melting/solidification effects. Phase-change heat transfer will be treated using the enthalpy method. The effect of different PCM configurations on thermal performance will also be studied.

The improvement in performance using PCMs will be compared to baseline computations without phase change materials. Finally, suitable PCM candidates (n-paraffins), and their desirable applications in specified requirements, will be identified. Experiments are planned to validate the computations. For more information, please contact Dr. Yogi Joshi at (301) 405-5428.

Phase Change Material Slurry

As a follow-on to previous work in liquid cooling of electronic components, testing is in progress on a slurry formed from a micro-encapsulated phase change material (PCM) suspended in oil. The phase change material, octadecane, is sealed inside a polymer shell, forming capsules 10-80 æm in average cross section. The oil is a 80/20% mixture of PAO and CTFE, both synthetic oils. The mixture is used to achieve a fluid density that matches the overall density of the phase change capsules.

The PCM scheme is considered important by the U.S. Air Force, since weight and space savings associated with the reduced flow rates of the coolant are made possible by the PCM. In the study, the heat transfer characteristics of the PCM slurry are being investigated in flow-through SEM-E (standard electronic module, size E) configurations. It is expected that the higher effective Prandtl number (momentum diffusivity divided by thermal diffusivity) of the PCM slurry will yield significantly higher heat transfer performance than the oil alone. This will be an additional advantage beyond the system benefits that the Air Force is currently anticipating. For more information, please contact Dr. Keith Herold at (301) 405-5268.

Connector Reliability

The CALCE EPRC is continuing its connector reliability modeling effort, with active support from AMP and Bellcore. To support this effort, an Automated Contact Resistance Probe (ACRP) is now being built at the CALCE EPRC that will enable accurate measurement of contact resistance and deeper insight into the physics of contact surfaces in a connector. Using data acquisition hardware and software, the ACRP will be used for real-time contact resistance measurements of plated coupons and connector samples. Some of the features of this new ACRP "super-probe" include normal force variation from 0 to 1000 grams, with an accuracy of ñ 0.3g at a rate of less than 2g per minute, using a hydraulic arrangement; an x-y motion table with a resolution of 0.254æm or less, enabling contact resistance

measurements to be taken at specific points on a coupon sample; and a precision power source providing source current from 1nA to 1A and source voltage from 0.1mV to 110V, with a resolution of 10æV, to enable accurate contact resistance measurements.

In addition to contact resistance measurements, the CALCE EPRC will be conducting porosity tests using low-pressure nitric acid vapor on gold-plated samples. The results will be used to correlate porosity with contact resistance. For further details please contact Rod Martin at (301) 405-5325.

Surface Mount Capacitor Reliability

The reliability of multiple-layered ceramic surface mounted capacitors (MLCCs) has historically been problematic, due to environmental stresses introduced during wave soldering and product use. One significant problem is the formation of internal cracks during the soldering process. Generally, temperature gradients and differential thermal expansion of the metal electrode and the ceramic induce thermal stresses in the ceramic. The fabrication materials play a key role in determining the stresses created during thermal shock and thermal cycling; they also influence the probability that a crack will form as a result of these stresses.

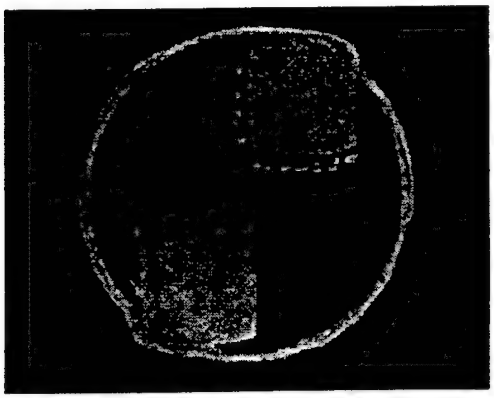
The goal of this project is to develop mathematical models that can be used to assess the manufacturing issues and associated reliability of MLCCs, based on physics-of-failure methods. The objectives are to identify relevant product design variables; identify relevant environmental stresses; use finite element analytical techniques to evaluate stresses; identify relevant failure modes; perform design-of-experiments on finite element models to derive closed-form models; and incorporate the mathematical models into the CALCE software. For more information, contactDr. Pat McCluskey at (301) 405-0047.

Through-hole Connectors

Reliability issues related to soldered interconnects have prompted several manufacturers to investigate the use of through-hole solder-less interconnects. AMP and the CALCE EPRC are jointly involved in establishing critical quality standards for spring loaded through-hole connectors, since pin- insertion forces cause damage to the surrounding plated through-hole (PTH) and board (see figure in right column).

The traditional method of assessing damage involves cross sectioning and observing microscopically each new configuration and each new lot. The CALCE EPRC is now developing analytical models based on fundamental physics-of- failure principles to provide alternative methods of assessing the magnitude of damage caused and establish acceptance standards.

The models will be verified using an extensive database collected by AMP. Establishing validated models will result in significant cost savings, because the need for experimental characterization of damage will be eliminated. This is an example of how physics-of-failure simulation techniques are being utilized to minimize hidden factory costs. For more information, please contact Dr. Abhijit Dasgupta at (301) 405- 5251.



Through-hole connector cross section with PTH damage

Accelerated Testing

The CALCE EPRC is developing software for accelerated test guidelines based on the physics-of-failure approach. Tests and screens are usually selected from government/military specifications, such as MIL-STD-883, in the hope that the stresses and stress magnitudes will target dominant failure mechanisms and reveal the suitability of a technology or design for a given application environment. However, as noted by the Air Force Rome Laboratory, in the Spring IEEE Reliability Newsletter, "Although manufacturers continue to use these screens today, most of the screens are impractical or need modifications for new technologies, and add little or no value for mature technologies. . . . With the defense budget/market declining, the DoD cannot afford costly test requirements that add little value to product quality or can be met in other ways."

The new testing approach determines test levels based on failure mechanisms, failure modes, and stresses for the application. It uses quantitative failure models and acceleration transforms, and adapts the knowledge of dominant failure mechanisms to the selection of accelerating stress parameters. The stress levels, designed specifically for each test article, are based on manufacturing processes, geometry and materials. For more information, please contact Dr. Pat McCluskey at (301) 405-0047.

Electro-optics Physics-of-Failure Project

The CALCE EPRC has been developing a physics-of- failure approach for the reliability assessment of microelectronics. With funding from the Department of Defense, this approach will now be extended to include electro-optics. A project team consisting of U.S. Army organizations and the CALCE EPRC will initially evaluate uncooled focal plane arrays and solid state YAG lasers. The planned project activities include:

- identification of potential failure mechanisms, failure modes, and failure sites;
- identification of failure mechanism models;
- identification of pertinent materials and their characteristic properties;
- development of physics-of-failure software tools;
- validation of approach through experimentation and simulation;
- development of project documentation and software documentation; and
- coordination of government and industry workshops for communication of research results.

For more information, please contact David Mortin at (410) 278-2153.

New Electromigration Book

Electromigration and Related Electronic Device Degradation, edited by Dr. Aris Christou.

Created: 5/21/95 Updated: 11/10/95

CALCE News

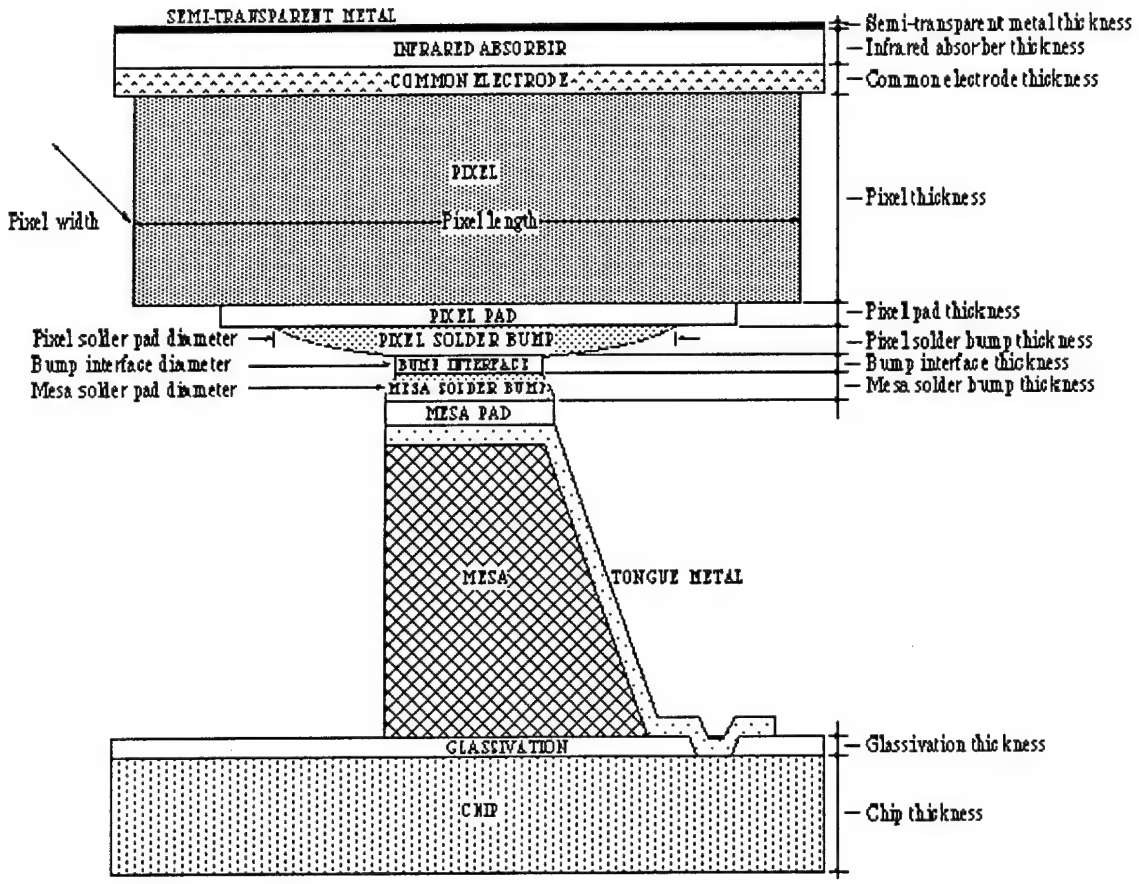
September 1994

Reliability of Uncooled Infrared Sensors

The advent of uncooled infrared sensors has created an opportunity to achieve a low-cost night vision sensor. Traditional infrared sensors use photon-detecting technology that requires cryogenic operating temperatures to reduce the intrinsic electrical no ise.

The Texas Instruments Uncooled Focal Planar Array (UFPA) is a new infrared detector that utilizes the electric properties of Barium Strontium Titanate (BST), operated under constant bias, to detect infrared radiation; it does not require cryogenic cooling . The infrared radiation absorbed by an optical coating in intimate thermal contact with the BST element induces a temperature change causing a variation in the polarization and capacitance of the material. This is sensed as a volatge fluctuation. To form an image, a planar array of BST elements (or pixels) is used to collect incident radiation over a given area; the base of the array is kept constant at 23 degrees Celsius using a thermo-electric cooler. Resolution of the infrared image is dependent on th e temperature gradient through the structure. The thermal effect of the incident infrared rays on the surface of the array determines performance and its subsequent effect on the reliability of the assembly.

The CALCE EPRC has used the physics-of-failure approach and finite element modeling to develop software tools to assess UFPA reliability. The software uses a coupled global-local finite element method to assess the thermal and thermo-mechanical response. Modifying dimensional and material parameters allow alternative designs to be evaluated. For more information, please contact Dr. Don Barker at (301) 405-5264.



Uncooled infrared focal planar array model.

Knowledge Based Design Advisor

The CALCE Electronic Packaging Research Center (EPRC) is developing a knowledge based design advisor to capture electrical based design knowledge for future incorporation by Computer-Aided Engineering (CAE) vendors to advance industry availability of "tur n-key" knowledge based tools. A knowledge-based computerized system uses knowledge about a specific domain to solve a problem in that domain. The solution is essentially the same as would be concluded by a person knowledgeable about the domain if confront ed with the same problem.

The project targets the rules for circuit design, schematic capture, and part list generation. So far, design rules have been captured from the following groups:

- Honeywell
- NASA
- EDS
- Texas Instruments
- MIL-STDs
- PreAmp
- the University of Maryland.

The project is being sponsored by the Reliability and Maintainability Symposium (RAMS) Council for

Reliability, Quality, and Competitiveness. The CALCE EPRC is a core team member, working on rule capture and implementing the rules in the database. For mor e information, contact Joan Lee at (301) 405-5323.

Material Characterization CRADA

The CALCE Center has developed and maintains a materials database that includes the common electronic packaging materials for zeroth, first, and second level electronic packaging. The software includes mechanical, electrical, and thermal properties of mat erials and capabilities for including property dependencies on temperature, frequency, moisture, altitude, and processing conditions.

To refine and standardize the methods used for characterizing the behavior of packaging and interconnect materials and structures currently used by the U.S. microelectronics industry, the CALCE EPRC has entered into a Cooperative Research and Development Agreement (CRADA) with NIST, IBM, Delco, Digital Equipment, Texas Instruments, Motorola, DuPont, Dow, NASA-JPL, DoE-Sandia, and Navy-Crane. The objective is to create a forum on advanced microelectronic packaging and interconnect material meteorology.

The forum will consider technical advancements needed in materials measurements and standards to support the data quality and availability requirements of U.S. microelectronic packaging and interconnect designers, manufacturers, and reliability assessors of high volume commercial products. Measurement parameters include electrical, thermal, mechanical, physical, interfacial, and chemical properties and the meteorology for determining time to failure. For more information, contact Dr. Michael Pecht at (301) 405-5323.

Accelerated Testing of Surface Mount

A study has been initiated to illustrate how the physics-of-failure approach can be used to achieve test-time compression for cost-effective qualification testing. Previously, determination of acceleration transforms to relate test data to field reliabili ty required multiple temperature cycle profiles. Now, using physics-of-failure models, acceleration transforms can be derived from just one temperature cycle profile.

As part of this study, the CALCE EPRC recently conducted accelerated temperature cycle tests on leadless surface-mount components. Components of various sizes were mounted on printed wiring boards (PWBs) with various coefficients of thermal expansion (CTE). Leadless solder joints typically fail due to fatigue under temperature cycling; the driving stress is the thermal expansion mismatch between the component and the PWB. The effect of components size and PWB CTE on solder joint stresses is theoretically estimated from a physics-of-failure model for low-cycle solder joint fatigue [IPC-SM785]. Thus, tests at a single temperature history effectively provide a large database for obtaining acceleration transforms.

The acceleration transform curve for a 68 pin leadless chip carrier (LCC), assuming a Weibull distribution at 5% probability of failure, is presented in the figure below. The discrepancies between the experimental data and the theoretical acceleration tra nsform (predicted by the IPC model) are symptomatic of the limitations of the current IPC model for accelerated testing, especially at temperatures below 20 degress Celsius.

Future work will employ a more detailed physics-of-failure model (the CALCE EPRC energy partitioning model) to quantify the experimental results. For more information, contact Dr. Abhijit Dasgupta at (301) 405-5251.

Acceleration transform for 68 pin LCC.

CADMP-II Software v1.0 Released

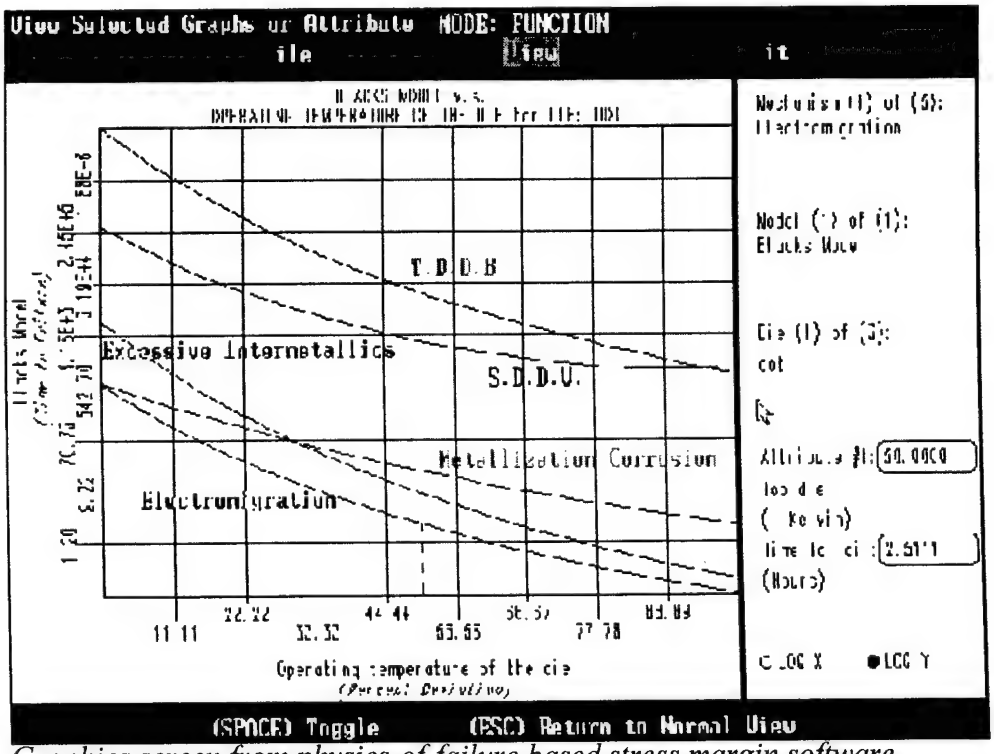
The CALCE EPRC has released version 1.0 of the CADMP-II (Computer-Aided Design of Microelectronic Packages) software. The software has been tested at eighty alpha and beta sites over a period of two years and is supported by the members of CALCE EPRC. New additions to the software include:

- ***Stress Margin SoftwareTools:***

  Physics-of-failure based stress margin software tools (see figure below), developed as a part of a project with Semiconductor Research Corporation, have been integrated into existing modeling/design frame works of the CADMP-II software. The tools have been developed to address the derating of electronic packages. The CALCE EPRC, however, prefers to use the word "derating" with caution. Over the years, the term has been misused to reduce equipment operating temperature in the name of reliability. Studies, however, have shown that lowering temperature may not increase reliability [Kopanski 1991, Lall and Pecht 1992, Witzman 1991], and substantial costs are associated with lowering temperature. Derating, prop erly employed, is a science-based technique through which operating parameters on a component are modified to enhance reliability. Typical derating parameters include junction temperature, voltage, current, and frequency, depending on the device type.

- ***Accelerated Testing Tools:***

  Accelerated testing tools based on physics-of-failure concepts developed at the CALCE EPRC have been added. The approcah involves incorporating knowledge of dominant failure mechanisms into the selection of accelerating stress parameters. The stress levels will be design specific, based on the geometry and materials. A proactive environment has been provided to facilitate the evalution of trade-offs between various stresses that accelerate a given mechani sm or mode.



Graphics screen from physics-of-failure based stress margin software.

- ***MIL-STD-1835 Naming System:***

Each package modeled can automatically have a name assigned to it based on the Military Standard 1835 package descriptive designation system.

- ***Package Attribute Definitions:***

  All attributes of the package design are now explicitly defined with figures. The definitions, drawn from scientific and technical dictionaries, books, handbooks, articles, and CALCE EPRC research, allo w exact representation of the designated value. This has been provided in response to requests from the beta sites for clearer definitions of package attributes.

- ***Failure Model Verification Tables:***

  These tables list and describe all of the variables, submodels, and models that are used for package analysis, including the actual equations.

For more information about the CADMP-II software, contact Richard Bauernschub at (301) 405-5329.

System Level Thermal Control Simulation

In the past, empirical methods have been used to analyze the cooling design of electronic systems. More recently, simulation using computational fluid dynamic (CFD) techniques have been developed, thereby providing an opportunity to reduce product cycle t ime and total cost by eliminating unnecessary experimental testing.

To validate the application of CFD simulation for complex electronic systems, the CALCE EPRC and Loral Federal Systems Division (Manassas, VA) are comparing simulation results with experimental test data. The electronic system being analyzed is a chassis of commercial VME boards using forced convection air cooling. FLOTHERM, a finite volume-based CFD software package specifically for analyzing heat transfer of electronics, is being used as the simulation tool.

A diagram of the computed flow vectors in a plane parallel and adjacent to one of the VME boards is shown below. The flow shows large recirculation zones with very little air flow, which results in inadequate cooling of some components in these regions.< P> The simulation results are in general agreement with measurements on the actual system. Simulation models are now being used to study the effects of different chassis modifications to acheive more even air flow distribution. For more information, contact Dr. Yogi Joshi at (301) 405-5428.

Computed flow vectors of forced air over a VME board.

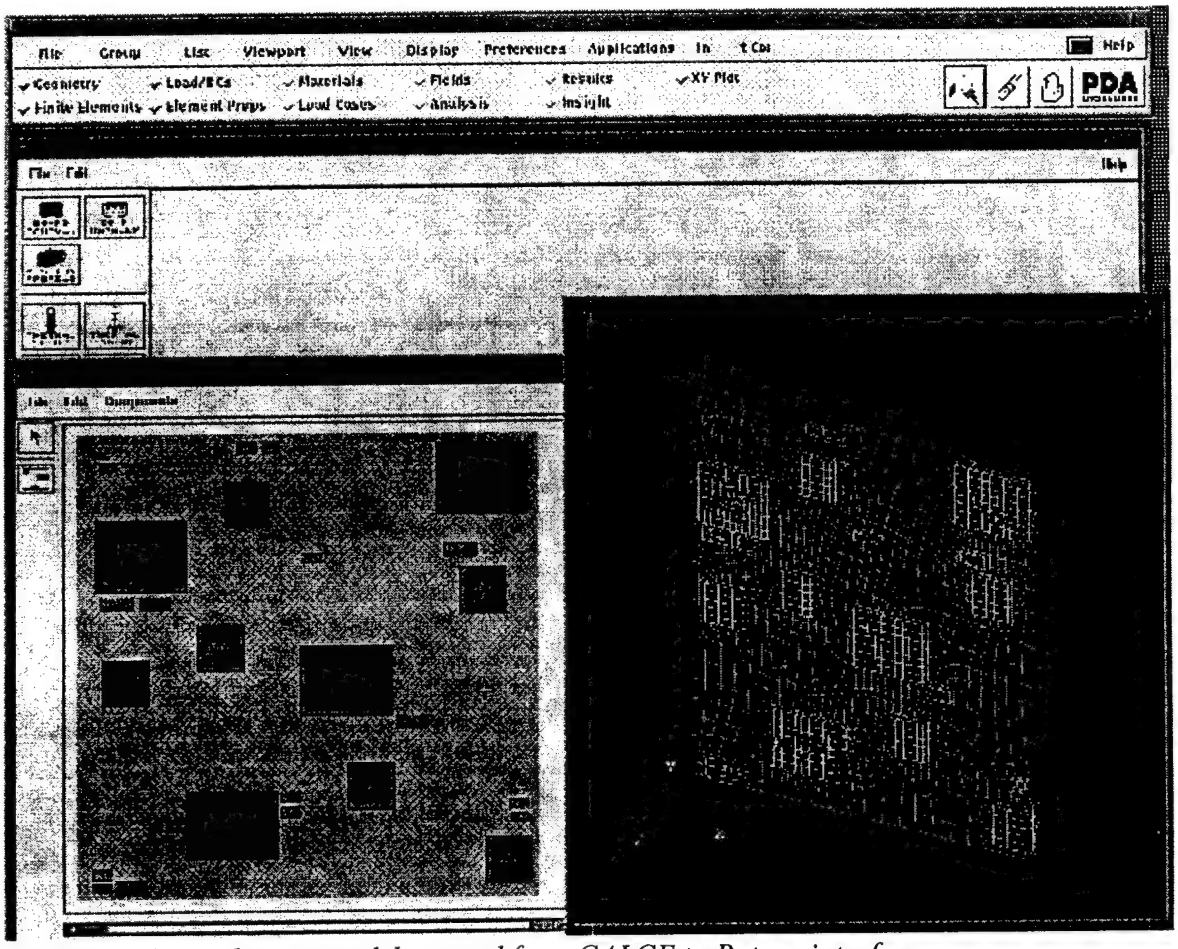
Patran Interface

The CALCE Unix Software now has the capability to interface to Patran finite element modeling and analysis software from MacNeal-Schwendler Corporation. Patran permits detailed thermal and vibrational analysis of electronic packages.

Using CALCE import/export utilities and Patran command language (PCL), the interface automatically exports the CALCE board model and constructs a Patran model. The model imported from CALCE is meant to be the first stage in a two stage modeling process.

In the first stage, components are represented by cuboids that model the dimensions of each individual part. In the second stage, areas of interest identified in the first stage, such as leads and solder joints, are modeled in more detail. Results derive d in the first stage are also used as boundary conditions for second stage analysis.

This technique limits the analysis scope to a manageable size and reduces required computer resources, while pointing out areas that warrant further investigation. For more information, please contact Michael Osterman at (301) 405-8023.



Display of finite element model created from CALCE to Patran interface.

Created: 5/21/95 Updated: 11/10/95

CALCE News

February 1995

Electronics at Elevated Temperatures

Many benefits can be derived from operating sensor and control systems at temperatures above 125 C. Operation at higher temperature permits these systems to be placed closer to the environments they monitor, such as automotive and aircraft engine controls. This minimizes the cost, signal degradation, and reliability concerns arising from cooling systems, long cables, and other system modifications designed to keep control electronics cool.

Developments in the design and manufacture of electronic components indicate that the currently accepted temperature limits of -55 C to 125 C may be unduly restrictive. Many systems should be able to perform adequately up to 200øC with no changes. In other cases, system failures could be avoided by selecting different materials or varying design parameters to accommodate higher steady-state temperature use. For example, conductive filament formation in FR-4 boards can be minimized at high temperatures by choosing either a wider conductor spacing, a lower operating voltage, or a more moisture-resistant laminate system.

The CALCE EPRC is conducting a two-phase study to identify the technical challenges involved in operating systems at elevated temperatures. The first phase focusses on collecting and analyzing material data for temperatures up to 200øC, including mechanical, electrical, and thermal properties, and their relationship to temperature within that range, are being assessed. The most important properties for system operation and reliability are being emphasized. At the completion of the first phase, a report on the temperature dependencies of material properties for each packaging element will be available to CALCE EPRC members.

The knowledge gained in the first phase will be used in the second phase to evaluate six candidate electronic hardware designs for a wide range of modules, each of which contains multiple components, cards, and associated hardware. Each system will be evaluated on the basis of its parts list, which includes information on the device technologies, the package family types, the assembly and interconnect materials, and the board constructions. In addition, actual units and assembly drawings will be used to determine the locations of the parts in the system. The materials-related concerns that arise in these systems at high operating temperatures will be identified, together with strategies for accommodating elevated temperature use through materials selection and design variation. For more information, please contact Dr. Patrick McCluskey at (301) 405-0047.

Popcorn-free Manufacturing with PEMs

Delamination and popcorning are failure mechanisms that occur when plastic encapsulated microcircuits (PEMs) are assembled onto circuit cards by solder reflow. Though the devices may pass electrical (and other) tests initially, cracks in the encapsulant could facilitate the ingress of corrosive contaminants and lead to catastrophic failures while the device is in use. Full-blown cracking can also result in the shearing of wirebonds and immediate failure.

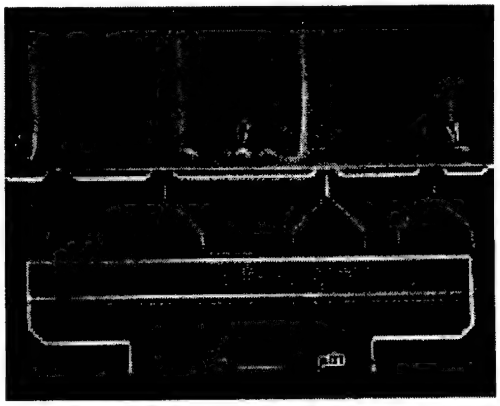
The temperature ramp rate used during reflow is a critical process parameter affecting the occurrence of delamination and cracking. The magnitude of the stresses generated in the PEM due to mismatches of the coefficients of thermal expansion (CTE) at the interfaces and the presence of moisture will be lower if lower temperature ramp rates are used. The lower ramp rates also facilitate the efficient desorption of

An environmental scanning electron microscope (E-SEM) works with specimen pressure chambers ten thousand times higher than that of the traditional SEM, without contaminating the microscope. This pressure condition allows examination of unprepared, uncoated specimens in their natural environment. Dynamic characterizations of wetting, drying, absorption, melting, corrosion, and crystallization can also be performed.
The E-SEM at the CALCE EPRC has the following unique capabilities that permit in-situ evaluation:

- Environmental pressure control system in which the pressure source can be selected from among water vapor, air, argon, nitrogen and other gases;
- Temperature substage in the environmental chamber, plus a temperature control system set-up enabling changing the temperature of a specimen in the range of -196o C ~ 400o C with a programmable rate;
- Mechanical test substage with tensile, compression, four-point bending and shear modes, and a load control system ranging from 1 g ~ 450 kg; and
- Micromanipulator and fluid injector that can supply various chemical solutions on the specimen during E-SEM operation, allowing the characterization of corrosion resistivity of the specimen.

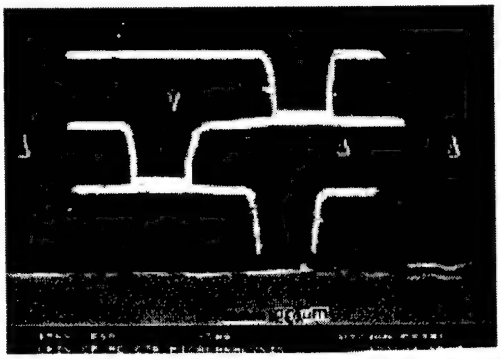
The following are examples of electronic packages dynamically investigated using E-SEM:

1. *Transimpedance amplifiers:* Surface defects due to reactions between the polyimide film and metallization were observed after temperature cycling using a temperature substage. The GaAs chip was passivated with a 10æm thick polyimide film for protection from environmental contamination. Previous investigation indicated a low mean time to failure at temperatures above 200oC. When the temperature increased to 180oC, the polyimide film started to degrade. Several interfacial defects, such as a hillock, formed as the temperature reached 220oC.



1) Transimpedance amplifiers: Surface defects due to reactions between the polymide film and metallization.

2. *High-density interconnects (HDIs):* HDIs, used in multichip modules, were examined after relative humidity (RH) cycling. Polyimide/metallization debonding and polyimide/polyimide delamination were observed.



2) High-density interconnects: The third arrow points to an area of polymide/metallization debonding and the first, second, and fourth arrows point to areas of polymide/polymide delamination.

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CALCE News

August 1995

Timely Product Development

When one examines the key issues to competing in the global market, cost is clearly one of the major considerations. Developing products that cost less is a prime goal which impacts the design and development of a product. However, if the product is not available to the market in a timely manner, the cost can be irrelevant. In fact, many CALCE EPRC members have found that about one-quarter of the market is gained by the company which is first to market the product.

So, how does one develop products in a more timely manner? The CALCE EPRC is conducting various research efforts to identify the bottlenecks and explore alternative methods and techniques to remove the time-delay barriers. As part of these efforts, the CALCE EPRC has been investigating product flows, with particular emphasis on the flow associated with product qualification and quality assurance. Our view is that most electronics companies do neither of these tasks particularly cost effectively or efficiently. For example, many companies still conduct Mil-Std-883 qualification tests and quality assurance screens which are impractical or need modifications for new technologies, and add little or no value for mature technologies.

The CALCE EPRC has determined various methods to reduce qualification and quality assurance time and ensure greater reliability. The foundation of these methods for microelectronics packages can be found in the book titled Quality Conformance and Qualification of Microelectronic Packages and Interconnections, John Wiley, 1994, edited by Michael Pecht and Abhijit Dasgupta from the CALCE EPRC and John and Jillian Evans from NASA, with contributions from some twenty industry, government and university experts.

Emphasis at the CALCE EPRC is now being placed on examining timely product assurance for specific technologies such as plastic encapsulated microcircuits, ball grid arrays (PBGA)s, multichip modules and printed wiring board assemblies.

CALCE EPRC Planning Meeting (October 26-27)
The Industrial Advisory Board will meet to cover administrative issues, plan for next year's research activities, and to distribute proprietary research findings. This meeting is open to members only.

Health Management of Electronic Systems

In the electronics industry, failure causes are often characterized as assignable causes and non-assignable causes. Assignable causes can be clearly analyzed in terms of failure sites, modes and mechanisms. On the other hand, non-assignable causes are classified as *can-not-duplicate (CND), retest-OK, cannot-verify*, or *unknown-causes*. In electronics, non-assignable causes are responsible for up to 70% failures, suggesting (1) incompatibility between testing and application environment (stresses, operating conditions, human interactions), (2) lack of information about the onset and cause of failure, and (3) intermittent and self-healing failure mechanisms.

Health management is an affordable, efficient, and reliable on-line, non-destructive technique that involves development of health monitors incorporating sensor technologies, heuristic, mechanistic, and stochastic on-line diagnosis algorithms, and physics-of-failure reliability assessment for in-situ defect detection and reliability assessment. The technique provides information about the actual stresses

responsible for failure and ensures compatibility of the test conditions with application environment. Health monitoring also enables early detection and warning of an imminent potential failure, critical in an electrical circuit, as it is the key to the safety of personnel and equipment. Finally, health monitoring enables higher operating efficiency to be achieved, because it provides information regarding the need for maintenance (repair or replacement).

Successful health management requires multiple integrated sensors for monitoring the physical condition of the electronic system. Accelerometers, strain sensors, stress sensors, resistive sensors, capacitive sensors, thermistors, all can provide needed sensory input. The data then must be analyzed, integrated and classified into a number of inference classes, and then coupled with computational algorithms capable of locating failure sites and predicting the extent of degradation.

Physics-of-failure approach is integrated with health management to estimate the remaining life of the system. The approach uses mathematical models based on the fundamental physical and chemical processes by which failure occurs. With these models, it is possible to estimate the time-remaining-to-failure using the information about stresses acting on the system, sensory inputs, relevant material properties, and original design. This methodology is enhanced by the use of health monitoring fuses. This involves incorporating on-line health monitors having design geometries that accelerate failure by a particular mechanism. The acceleration factor for a test structure is determined by the physics-of-failure models. This acceleration factor, together with the monitored time-to-failure for the test structure is used to estimate the time-remaining-to-failure of the actual part.

If you are interested in contributing to this activity, please contact Ms. Joan Lee at (301) 405-5323.

Long Term Storage Reliability of PEMs

Considerable effort has been expended in the past ten years characterizing the reliability of plastic encapsulated microelectronics (PEMs) under normal operating conditions. However, very little information is available on the effect of long term storage on future reliability. This information is crucial to making correct parts selection and design decisions for next generation products. In addition, the information is extremely valuable to users and distributors for replacement parts for existing products. To address these issues, the CALCE EPRC has initiated multiple efforts to analyze degradation in PEMs due to long term storage.

Through a cooperative research and development agreement (CRADA) with the Army Research Laboratory, CALCE EPRC is pursuing efforts to assess the reliability of PEMs on military Sonobuoys and unassembled PEMs stored for 8-12 years. A three phase approach is being used for this assessment. In the first phase, CADMP-II simulations are being conducted on the parts to determine the dominant failure mechanisms, modes, and sites, to guide the degradation analysis. This phase also includes the calculation of physics-of-failure based acceleration transforms for these dominant failure mechanisms. In the second phase, materials analysis techniques are being used to identify and characterize the degradation. This includes (1) using visual and optical microscopic examination to observe external cracks, corroded leads, or other signs of damage; (2) electrical testing to identify parametric shifts; (3) scanning acoustic microscopy to observe package delamination and cracking, and die attach voiding; (4) decapsulation and E-SEM/EDS to see evidence of corrosion, passivation cracking, electromigration, stress driven diffusive voiding, wire fatigue and fracture, and die cracking; and (5) cross-sectioning and E-SEM/EDS to characterize intermetallic growth. The degradation in stored PEMs is being compared to the degradation in ceramic parts stored for an equivalent period of time. These analyses are providing the first conclusive information on the location, mechanisms, and extent of degradation in PEMs caused by long term storage.

In the third phase, CALCE EPRC is addressing the critically important issue of estimating the "remaining life" of PEMs. This is being accomplished using a combination of the physics-of-failure models for the dominant failure mechanisms and accelerated testing on both the old and new components. The testing includes temperature-humidity stress tests, highly accelerated stress tests (HAST), and temperature cycling tests. The time-to-failure determined by these tests will be used

together with physics-of-failure acceleration transforms calculated in phase I to assess "remaining life" for PEMs in various storage environments.

If you are interested in contributing to this effort and in obtaining the results of these investigations, please contact Dr. Patrick McCluskey at (301) 405-0047.

CALCE EPRC Offers Services to Qualify PQFPs and PBGAs for Popcorning

Popcorning is a failure mechanism in plastic encapsulated microcircuits (PEMs), which occurs when the inherently hygroscopic encapsulant is rapidly exposed to high temperatures during reflow solder assembly of the component to a printed circuit card. Popcorning is characterized by the development of interfacial delamination and cracks in the encapsulant. Popcorning can lead to a long-term reliability problem, since the cracks may serve as a path for ionic contaminants, causing corrosion-induced failures. Further, popcorning may result in sheared or cratered ball bonds leading to electrical failures. Effective techniques to assess the susceptibility of PEMs to popcorning include the combined use of X-ray radiography and probe methods for the *real-time* investigation of the cracking phenomenon, followed by acoustic microscopy to quantify the extent of delamination and cracking, and electron microscopy to examine selected cross-sectioned devices.

Background

Epoxy molding compounds are hygroscopic; the ingressed moisture accumulates at the interfaces inside the PEM. During reflow soldering, the entire PEM is heated to temperatures as high as 230øC, well above the glass transition temperature of most molding compounds. Stresses are developed in the PEM as it is heated to reflow temperatures. The factors contributing to the stresses include the rapid vaporization of absorbed moisture resulting in the build-up of vapor pressure, thermal expansion mismatches at the interfaces of the PEM, and a decrease in the adhesive strength and fracture toughness of the molding compound. When the hygrothermal stresses and vapor pressure exceed the adhesion strength and fracture toughness of the molding compound, they become the driving forces behind the growth of the delamination and the formation and propagation of cracks.

Popcorning may not result in the immediate failure of the package. However, the long-term reliability of the package could be jeopardized if surface-breaking delaminations and cracks serve as a path for the entry of ionic contaminants into the package. Delaminations and cracks that do not appear externally can also lead to reliability problems. During temperature excursions, the delaminated plastic may be free to move relative to the die surface, possibly stressing and damaging passivation and metallization. Cracking and delamination between the molding compound and the die surface may also lead to sheared or cratered wires and ball bonds, causing immediate failure or intermittent electrical failures during temperature excursions. Information on PEM composition, reliability and qualification can be found in the book titled Plastic Encapsulated Microelectronics by Pecht, Nguyen and Hakim, John Wiley, 1995.

A test methodology to effectively assess the susceptibility of PEMs to popcorning

The test system designed, built, and in-production use at the CALCE EPRC, consists of an X-ray radiography unit and probe tester embedded in an infrared heating system. The PEM can be precisely heated through any desired infrared reflow temperature profile, while simultaneously monitoring its X-ray image and out-of-plane deformation, in *real time*, for popcorning. The video image of the X-ray is processed and displayed on a monitor and is recorded on video cassette or photographic film. The probe is set up against the face of the PEM, and is used to quantify the doming of the encapsulant prior to package cracking.

The equipment can be used to identify the specific stage of the reflow profile at which doming of the encapsulant and package cracking occurs. It is an effective tool to study the effect of variations in parameters such as reflow temperature ramp rates and moisture content of the device on popcorning in PEMs. The build-up of vapor pressure is responsible for the formation of the characteristic dome-shaped

bulge in the encapsulant. Popcorning is characterized by the growth of this bulge and eventual cracking of the device. The probe is used to physically measure the extent of doming that occurs in PEMs, as they are heated through the reflow cycle. The device thickness is continuously monitored, and the total deformation of the device just prior to cracking is detected with an estimate of the critical level of device doming, beyond which cracking occurs.

An acoustic microscope is then used to quantify delamination and popcorn cracks in PEMs. At the CALCE EPRC, we use the Sonix reflection-type microscope that generates images by mechanically scanning a transducer in a raster pattern over the sample. The transducer alternatively acts as sender and receiver. A very short acoustic pulse enters the sample, and return echoes are produced at the sample surface and at specific interfaces within the part. An oscilloscope display of the echo pattern clearly shows these levels and their time-distance relationships from the sample surface. Software converts this information into a pseudo color map of the sample interface. The contrast of the image is due to the acoustic impedance mismatch of the different materials at the interface. The image is used to quantify the extent of delamination, in terms of percentage area.

In some cases, such as with PBGAs, selected devices are cross-sectioned and examined using an environmental scanning electron microscope (E-SEM), in order to confirm the results obtained. The E-SEM can be used to study materials under controlled environmental conditions. The advantage of using an E-SEM is that uncoated specimens, free of surface charge and high vacuum damage can be examined. For information on service costs, please contact Joan Lee at (301) 405-5323.

Electronic Equipment Physics-of-Failure

The U.S. government has found that many companies that supply to the military and the government-regulated avionics, nuclear and space industries, have been constrained by the set of standards, specifications, and handbooks. Such constraints have resulted in a unique government/military electronics industry burdened with expensive customized parts, costly procurement procedures, lengthy paperwork, increased time to market, and reduced reliability.

With support from the Deputy Under Secretary of the Army (Operations Research) and the Office of the Assistant Secretary of the Army (Research, Development and Acquisition), the Headquarters of the Army Material Command authorized the Electronic Equipment Physics-of-Failure (EEPOF) project. Involvement is in the defense conversion and dual-use arenas, where physics-of-failure concepts are being used to revamp the reliability technologies associated with design, engineering, development, production, and life-cycle support.

Some key completed efforts include:

- the book titled Integrated Circuit, Hybrid and Multichip Module Package Design Guidelines: A Focus on Reliability
- the book titled Quality Conformance and Qualification of Microelectronic Packages and Interconnections
- prototyping of CADMP which lead to the development of CADMP-II and the CADMP-II Alliance
- Mil-Std-179 which reflects the PoF approach and enables CADMP-II to be used.

Currently under development are:

- An IEEE reliability program standard suitable for commercial-military dual-use that incorporates the physics-of-failure approach into reliability programs.
- An Electronic Equipment Physics-of-Failure Handbook that explains the application of physics-of-failure principles for electronic equipment design and manufacturing.
- Probalistic physics-of-failure methods.
- A science-based approach to developing field reliability estimates for logistical applications.

The impact of the EEPOF project will be to significantly reduce the time to design a test and highly reliable products. For more information, please contact Michael Cushing of AMSAA at (410) 278-2760 or e-mail: cushing@brl.mil.

Thermal Management of Portable Electronic Equipment

Thermal management is increasingly becoming important in the design of lightweight and compact portable equipment including laptop computers, miniature power supplies, pagers and cellular phones. To address this concern, the CALCE EPRC has been investigating the thermal characteristics of horizontally oriented PCBs in enclosures, of size simulating portable equipment. Of particular importance are the relative roles of conduction and convection in heat removal from the electronic components mounted on the PCBs. For horizontal PCBs in compact enclosures, the reduced air-space may under certain conditions inhibit air movement, resulting in conduction as the dominant heat removal mechanism. However, since convection can provide additional cooling, neglecting it in design calculations routinely may result in significant over-prediction of component temperatures. This can lead to unnecessary oversizing of the thermal management solution.

Certain key parameters have been identified which influence overall heat transfer most significantly for such problems. Numerical calculations and experiments to study the effects of these parameters and their interactions are in progress. General correlations for the maximum temperature within the components, as a function of the system physical parameters are also being explored. For further information, please contact Dr. Yogendra Joshi at (301) 405-5428.

Parts Selection

The CALCE EPRC is currently developing a parts selection/procurement flow chart to help increase early affordable access to state-of-the-art electronics technology in military and government applications. The decision making process includes:

- availability (vendor lead-time, multiple sources)
- supplier/distributor selection criteria
- obsolescence
- part cost
- type of package (fine pitch, ball grid array)
- standardization in terms of formats
- printed circuit board assembly manufacturing requirements, associated costs, and compatibility
- parts performance over temperature limits
- derating/stress margins needs and costs
- qualification methods and costs
- screening methods and costs
- application requirements (environments, performance)
- reliability (determination methods, requirements, cost)

Once the flow chart is completed, software will be developed to assist suppliers and customers in electronics design and assessment. If you are interested in supporting this effort, e-mail to: pecht@eng.umd.edu.

Created: 3/5/96 Updated: 3/5/96

CALCE News

February 1996

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10 Years as NSF Center of Excellence

In 1986, the National Science Foundation (NSF) awarded a grant to Professors Michael Pecht and Donald Barker to establish a center of excellence for electronic products research at the University of Maryland. As a result, the Computer-Aided Life-Cycle Engineering (CALCE) Center was organized as an Industry-University Cooperative Research Center (IUCRC). The thrust at that time was to address the life-cycle needs of electronics manufacturers.

In 1990, the name was changed to the CALCE Electronic Packaging Research Center (EPRC), with a focus on cost-effective, reliable electronic packaging. At that time, the CALCE EPRC was advanced to a State-Industry-University Research Center (SIUCRC), receiving a six-fold increase in funding from NSF, with matching funds from the State of Maryland and a tripling in industry sponsorship.

The technical direction concentrated on evaluating widely accepted reliability methods, including allocation, parts selection, reliability prediction, derating, environmental control, screening, and qualification. It became apparent that many manufacturers of electronic hardware had come to rely on the security of government-approved reliability documents such as Mil-Std-785 (*Reliability Program for Systems and Equipment*) and Mil-Hdbk-217 (*Reliability Prediction of Electronic Equipment*), even though following them often led to poor part selection, improper derating, high-cost cooling solutions, and long development times. Using these documents, any solution to a reliability question was deceptively simple: select specific devices, derate them, run them cool, and introduce redundancies. Auditing quality was accomplished similarly, with government mandated tests such as Mil-Std-883 (*Test Methods and Procedures for Microelectronics*), perpetuating the myth that reliability and quality could be tested into a product. The costs for following the mandated guidelines were passed on to the customer, resulting in more expensive products without a commensurate increase in performance or reliability.

Today, the CALCE EPRC has created an environment in which the technical limitations of industrial reliability practices have been identified and new, science based reliability guidance is being implemented. One significant outcome was the development of physics-of-failure reliability assessment software for printed circuit assemblies. This software has been used to evaluate avionics, automotive electronics, missiles, satellites, computers, power supplies, electro-optics, and communications equipment. It has also been commercialized by Texas Instruments and is available in their product called CARMA.

The CALCE EPRC is now implementing a fundamentally new approach to addressing reliability. Based on research into the mechanics of failure processes, knowledge of how failures occur is being gathered in order to gain control over failure mechanisms and manufacturing flaws. Coupling this data with novel simulation techniques, the CALCE EPRC is enabling design for reliability, reliability assessment, and virtual qualification (or qualification by design) of new electronic products.

One CALCE EPRC goal is to help our members develop highly reliable products ten times faster over the next five years

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Our approach and recommended procedures will impact all activities in the entire product development cycle, including basic system architecture, qualification, manufacturing, quality conformance, requirements for supporting sub-systems (i.e., cooling systems and redundancy), testing, and repair. The results will include significant cost reductions by eliminating previously hidden manufacturing costs, increased reliability of electronic systems, and quicker time to market.

Recognizing the critical competitive advantages of the CALCE EPRC approach, companies in electronics-related industries (avionics, consumer products, telecommunications, automotive) from all around the world are becoming members (see member list). With an annual research budget of over $4.5M and a team of over forty researchers, the CALCE EPRC and its members are aggressively preparing for the next ten years.

Laser Inspection System Donation

A Vanzetti Laser Inspection System was donated to the CALCE EPRC by Texas Instruments (Dallas, Texas). This inspection system for solder joints can significantly increase the productivity of assembly lines by eliminating visual inspection, and will be used to educate students, assist industry and government in research, and train factory-floor workers.

The Vanzetti system provides a single laser pulse to individual solder joints, examines its thermal emission, and through pattern-recognition algorithms, compares it to a known thermal signature of a good joint. The system can detect solder defects, such as insufficient and excessive solder, voids, damage, and bridging.

Near-term CALCE EPRC research will utilize the Vanzetti system for multi-beam laser soldering techniques. The advantages of laser soldering over conventional techniques include localized noncontact heating, desirable microstructure and mechanical properties, optimal intermetallic formation, and ease of automation. Application areas include opto-electronics and other micro-joining applications. The proposed investigations are particularly timely in light of the increasing interest in environmentally benign, leadfree soldering materials and fluxless processes.

A donation ceremony with representatives from Texas Instruments, the University of Maryland, and other dignitaries took place on November 20, 1995 (see photo below). Dr. Riccardo Vanzetti, inventor of the system that bears his name, attended the ceremony and gave a public presentation. For more information, please contact Ed Beatty.

From left to right: Will Willoughby (formerly of the Office of the Secretary of the Navy), Ricardo Vanzetti (Vanzetti Systems), Fred Henley (Texas Instruments), and Jim Raby (formerly of EMPF).

Ion Mobility In Molding Compounds

Moisture ingress into plastic packages can transport ions to the unpassivated bond pad area and lead to corrosion-related failures in integrated circuits. There is a high correlation between the concentration of halide ions in molding compound formulations and corrosion- related failures in plastic encapsulated microcircuits (PEMs), as well as a correlation between the concentration of antimony oxide flame retardant and the failure rate in PEMs. In addition, there is evidence in the literature that ion diffusion rates and failure rates may increase significantly due to additives in low-stress molding compound formulations. Despite the correlation between the concentration of ions and the failure rate in PEMs, an evaluation of ion diffusion rates in molding compound formulations has not been performed.

The CALCE EPRC is now conducting research to obtain a better understanding of the phenomenon of ion diffusion in PEMs and to assess the correlation between ion diffusion rates and failure rates in PEMs. To measure ion diffusion rates in epoxy molding compounds, researchers at the CALCE EPRC have designed an apparatus that incorporates a transfer molded block of molding compound as a semipermeable membrane separating aqueous solutions.

For example, the molded sample may separate an aqueous solution of sodium chloride (0.9% NaCl for salt water) from deionized water, and the diffusion rates of sodium and chloride ions may be measured by ion-specific electrodes. The electrodes, placed in both reservoirs to provide a mass balance for ion transport, are designed to detect ion concentrations in the ppb range. This technique has the advantage of measuring ion diffusion directly, rather than measuring changes in volume resistivity in the molded encapsulant as an indication of ion diffusion rates.

The dependence of the ion diffusion rate on the composition and cure schedule of the molding compound, ion size and charge, concentration of ions in the aqueous solution, and thickness of the molded encapsulant are being investigated. In addition, the dependence of the ion diffusion rate on temperature is also being examined to determine the effect of the high temperatures used for accelerated testing on diffusion rates and failure rates in PEMs.

These studies promise to fill a critical void in the literature on the ion diffusion rates in molding compounds and the relevance of molding compound composition and cure schedule to ion diffusion rates and failure rates in PEMs. With this knowledge, the reliability of PEMs in storage as well as operating conditions will be better understood. For more information, contact Dr. Michael Pecht.

Laser Diode Thermal Management Modeling

Many failure mechanisms in laser diodes are related to the operating temperature of the device. Consequently, thermal loading during operation has been the subject of many reliability studies.

The CALCE EPRC has developed a procedure to predict the temperature rise within the active region during operation. To begin, a simple heat generation model is used to allocate the power dissipation to specific regions and in specific quantities, as a function of the operating characteristics of the device.

A finite element analysis (FEA) has been applied to a commercial structure. The FEA was performed on a 2-D cross-section to generate the steady-state temperature profile in the active region during operation and the transient temperature response.

In conjunction, a design-of-experiments (DOE) approach was used to study the effect of a few operating parameters on the temperature rise in the laser structure. The DOE variables studied were thermal conductivity of the heatsink material, laser output power, and spacing between diode laser emitter elements. Statistical constants produced by the DOE analysis and physical relationships derived from application of fundamental heat transfer principles to our structure were then coupled to produce a simple analytical expression.

The expression will accurately reproduce the FEA result in predicting the maximum temperature rise within the laser emitter region. The expression includes the explicit dependence of the DOE variables studied on the temperature rise. The information gained can be used to make practical design choices and to ensure safe and reliable operation of laser devices. This approach can also be used in similar parametric studies and design evaluations. For more information, please contact Dr. Patricia Mead.

High Temperature Electronics TRP

The development of electronics that can operate at highly elevated temperatures has been identified as a critical technology for the next century. To address this issue, the CALCE EPRC is teaming with United Technologies, AlliedSignal, Boeing, Pratt & Whitney, Honeywell, Moog, Ford, Rockwell, Hamilton Standard, Parker Hannifin, Toranga Technologies, and others on a government-funded Technology Reinvestment Project (TRP). The objective is to develop high temperature electronics for integration into military/aerospace and commercial/industrial systems resulting in improved affordability, reliability, and performance. Leveraging previous and current efforts, the CALCE EPRC is contributing reliability assessment methods and software tools to meet the objectives of this high temperature electronics project. For more information, please contact Dr. Patrick McCluskey.

Optoelectronic Reliability Assessment

Traditional reliability assessment methods based on statistical curve fitting of failure data have typically been used in reliability prediction for commercial and military optoelectronic systems. However, because the optoelectronics industry is experiencing rapid change and improvement in manufacturer processes, standard failure data is often statistically insignificant or overly vendor-specific, thus highly inaccurate.

The CALCE EPRC has conducted a study of the reliability of laser diodes (LD), light emitting diodes (LED), and fiber optic cables. As a result, an outline of the major failure mechanisms for LDs/LEDs and optical fibers, and a discussion of the physical principles and environmental factors influencing the degradation process, has been produced. The study also identified some failure mechanisms (bond failure, electrode degradation, electromigration, and electrostatic discharge) that are common between LD/LED and microelectronic devices.

The study identified a great deal of work on the effect of fiber optic reliability on the characterization of silica (or plastic) fiber cable and the processes related to crack growth. However, research on the reliability and performance of assembled fiber connectors remains largely in the infant stages.

The study established that much of the previous work on failure mechanisms unique to optical components has focused almost exclusively on the impact of temperature and, in the case of optical sources, current density. Consideration of factors such as humidity, temperature cycling, mechanical stress, and material properties has typically been given only a qualitative treatment. This particular shortfall in the current research on optoelectronic reliability physics is an area in which the CALCE EPRC plans to have a significant impact.

The CALCE software was recently used to assess the reliability of a laser transmitter module that features a pigtailed optical fiber for output coupling of the laser signal. Algorithms for fiber optic coupling loss were applied following the calculation of vibrational resonances, which yielded component displacement values. Also, an acceleration factor for laser lifetime was determined, based on the calculated steady-state junction temperature under operation.

This software assessment highlights the necessity to treat optoelectronic reliability in a hybrid manner. The knowledge learned from assessing the typically silicon-based laser driver circuitry is quite important. However, the rudimentary treatment for assessment of the laser component and the fiber cable assembly is currently underdeveloped. One future CALCE EPRC goal is to improve the usefulness of our software tools for reliability assessment of optical components and systems typically found in optoelectronic systems. For further information, please contact Dr. Patricia Mead

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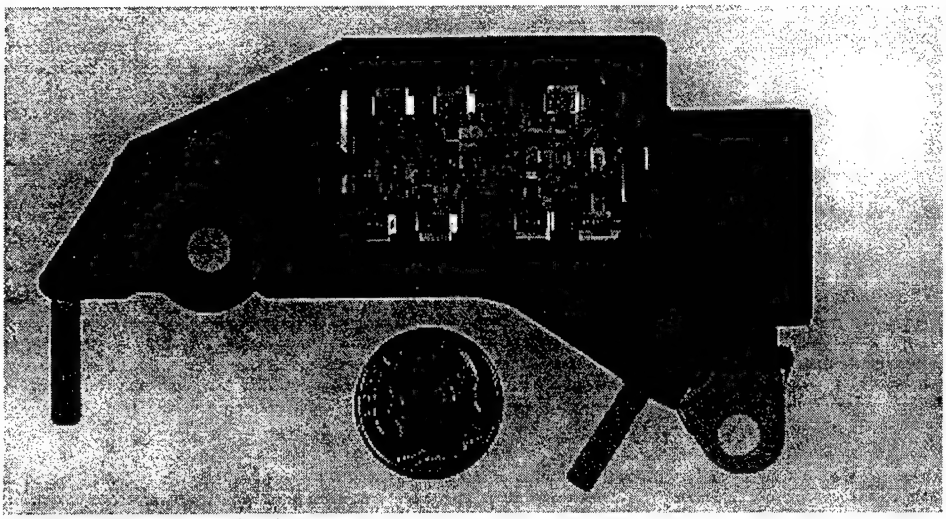
CALCE EPRC Efforts in High-Temperature Electronics

The development of electronics that can operate at elevated temperatures has been identified as a critical technology for the next century, and initiatives in this area are currently being pursued by many avionics and automotive electronics companies and their suppliers. Traditional limitations on the operation of electronic devices at temperatures above 125°C hinder the development of distributed control systems, smart sensors, and remote actuators, and increase the cost of electronic systems used t o monitor automotive, aerospace, and chemical process environments. The costs are a result of the additional size, weight, expense and reliability risks related to remote placement or cooling of these assemblies.

Advances in the design and manufacture of electronic components have made it possible to develop electronic systems that will operate reliably above the traditional temperature limits. However, successful development efforts hinge on a firm understanding of the issues related to semiconductor physics and device processing, materials selection, package design, and thermal management. The faculty of the CALCE Electronic Packaging Research Center (EPRC) have conducted extensive research on these topics, whic h will culminate in the publication of the first text of high- temperature electronics to address these issues.

This existing knowledge base, combined with the latest analytical and modeling capability and the world's only physics-of-failure based electronic packaging design-for-reliability toolset, makes the CALCE EPRC uniquely qualified to perform analyses and ev aluations of electronic systems for use at elevated temperatures. In fact, the ***CALCE EPRC was recently chosen to conduct all the elevated temperature reliability assessment involved in the development of the first commercially available 225°C d istributed control systems an effort supported by ARPA and fourteen major industrial participants, including United Technologies, AlliedSignal, Honeywell, Boeing, Parker, Moog, Rockwell, and Ford.***



The CALCE EPRC has developed an approach to analyzing electronic subsystems for use at elevated temperatures that has been utilized in assessing the viability of a number of different modules for Boeing, Delco, Honeywell, Eldec, AMP, and other members. Those wishing further information should contact Dr. Patrick McCluskey at : telephone (301) 405-0047, fax (301) 314-9269, or e-mail mcclupa@eng.umd.edu.

CALCE EPRC Receives NCMS Award to Study Lead-free Solders

The CALCE EPRC has been awarded a contract to develop life prediction models for lead-free solder alloys for the National Center for Manufacturing Sciences, (NCMS).

The objective of this study is to develop models for four lead-free solder materials based on data provided by NCMS from temperature cycling tests of 44-pin PLCC component assemblies. The CALCE EPRC will evaluate the thermo-mechanical durability of these materials using an energy-partitioning approach: CALCE's standard method of analysis includes studies of this nature. The model parameters for implementing the energy-partitioning model will be evaluated for all materials using the NMCS experimental data.

Deliverables for this project include software designed to perform the reliability analysis of these lead-free solders, as well as a database containing these new alloy material properties. Included will be the results of all finite element analyses used to evaluate model parameters. Also, all supporting equations and supplementary information required to explain the energy-partitioning model will be noted.

For more information please contact Dr. A. Dasgupta at (301) 405-5251 or e-mail: dasgupta@eng.umd.edu.

CALCE Optoelectronics Group Now Focusing on Adhesive Epoxies for Fiber Optic Applications

After a series of meetings between CALCE faculty member Dr. Patricia Mead and representatives from Tra-Con, Incorporated (Medford, MA), the Naval Surface Warfare Center (Dahlgren, VA) and Bellcore (Morristown, NJ), the core project in fiber optic connecto r reliability (FOC) is now focusing on characterizing the role of adhesive epoxies in FOC reliability. Industry-wide concern in this area was also expressed at the Telecommunications Industry Association (TIA) Committee Meeting on Fiber Optics held this p ast June in Quebec City, Quebec.

A collaboration with adhesives producers, connector manufacturers, and an end-user organization has been cultivated and a combination of three experimental procedures has been developed, including (1) measurement of fiber cable expansion/contraction chara cteristics during environmental cycling, (2) measurement of fiber cable stresses using a unique intrinsic fiber-sensor technique currently being

developed by the CALCE Optoelectronics group, and (3) characterization of currently available adhesive epoxy m aterial parameters. A finite element analysis of the termination subassembly within a MIL-28876C FOC has also been initiated in parallel with our experimental activities. Available results of these studies will be presented at the annual CALCE meetings th is coming October. TRW (Sunnyvale, CA) and GEC-Marconi are supporting this work. For further information contact Dr. Patricia Mead at: telephone (301) 405-0079, fax (301) 314-9269, or e-mail ashaki@glue.umd.edu.

Ruggedization of Laptop Computers for Mobile Applications

Portable computers provide the capability to access, retrieve, and store vast amounts of information, both locally as well as with other host systems, through wireless LANs and modems.

CALCE has worked to develop and bring to market a ruggedized mobile computing system, which is not only cost-effective, but also adds less than 20% to the weight and form factor of the originally manufactured equipment (OEM). The entire design cycle for this system was accomplished in a few months so as not to miss the optimum market window.

The ruggedization equipment will be mounted in the vehicle and be detachable for use outside the vehicle. It must have the capability to allow the OEM to withstand rain, dust, dirt, and spills in the keyboard; leakage through other openings; drops and sh ock loads; road vibrations; and extreme temperature variations.

A large segment of the portable computer market can be captured by ruggedizing versions of extremely popular and market-accepted IBM products to environmental survival characteristics, which exceed those of products currently available.

Currently, the IBM 730T and IBM 365 units are being experimentally ruggedized, and these attempts will be followed with further attempts on a series of other IBM computers and peripheral devices.

The key steps in the approach to ruggedize the 730T pen-based computer and the 365 laptop were to (1) perform simulation and early laboratory environmental testing on the unruggedized products to identify critical design issues for each product; (2) asses s various packaging options to develop a conceptual design capable of accommodating future IBM products not yet released; (3) turn the conceptual design into a final design for production; (4) conduct the necessary accelerated life tests on the final prot otype to validate the reliability of the final design; and (5) quantify the warranty risks.

The work accomplished, so far, has been to conduct thermal life testing (still in progress) on the ruggedized 730T units. Additionally, population reliability predictions were determined using a Chi-square distribution. Also, a conducted accelerated life vibration test is being done on 730Ts using scaled PSD profiles of rough road conditions to determine survivability. The results of these tests have fallen within one standard deviation of the mean. Further tests were done to determine the impact isolatio n characteristics of different boot materials for the 730Ts by subjecting them to various drop loads in order to identify and address all critical design issues for the 365 laptop. Additionally, a completed final design layout for the ruggedized unit that addressed all manufacturability issues was decided upon. For further information contact Dr. Donald Barker at: telephone (301) 405 5264, fax (301) 314-9269, or e-mail dbarker@eng.umd.edu.

Electronics Products and Reliability (EPAR) Study Program for M.S. and Ph.D.s

The rapid research and technology advances taking place in electronics packaging and product development must permeate in a timely fashion into the engineering education curricula, in order to provide a pool of qualified engineers to the industry in the c oming years. This must be achieved through systematically transferring "just-in-time" state-of-the-art knowledge and exposure to ongoing research activities to the student population about to enter the industry. Due to the strongly interdisciplinary natur

e of electronic packaging, traditional engineering curricula do not include a well- structured academic program to cover these topics. ***With over $2M of Technology Reinvestment Program (TRP) funds, advice, and support from the CALCE EPRC industry mem bers and support by the University of Maryland to revamp the curriculum, a new undergraduate and a graduate educational program in electronic products and reliability (EPAR) are now available.***

The EPAR program addresses the generic areas critical for attaining more cost-effective and reliable electronic products. A wide range of dedicated and cross-disciplinary courses are complemented by extensive computer systems and laboratory facilities.

A framework of coursework, examinations, and research projects leading to M.S. and Ph.D. degrees is being put in place. In order to meet the coursework requirements for these degrees, introductory and specialized courses have been developed at three level s. The first-level core courses serve as the entry points into the graduate program. More focused courses are offered at the second and third levels. Students in the EPAR program are generally required to take half of the academic credits from these cours es.

Support from two TRP awards has been utilized in developing five graduate courses: Opto-electronic Packaging and Reliability, Plastic Encapsulated Microelectronics, Surface Mount Manufacturing, Packaging Issues for Extreme Temperature Electronics and Ther mal Management in Electronic Packaging. In addition, an undergraduate course on Introduction to Electronic Packaging Materials was also developed. All courses included guest lectures from industry experts. In addition to the courses, two textbooks have be en written under the TRP funding in the area of high-temperature electronics. The TRP sponsorship during the coming year will be used to develop a number of multi-media educational modules in support of the EPAR curriculum.

Graduates from the EPAR program have been extremely successful in the job market. This year alone, twenty-two MS and six Ph.D. degrees were awarded and all of these students have obtained jobs in the U.S. electronics industry, with M.S. and Ph.D. starting salaries averaging $50K and $65K, respectively.

For more information, please contact Dr. Yogendra Joshi at: telephone (301) 405-5428, fax (301) 314-9269, or e-mail joshi@eng.umd.edu.

Contact and Connector Studies

Cost and density have a significant impact on the way reliable connectors are designed. Connectors can no longer rely on thick layers of gold plating and stiff contact springs to maintain a stable, low-resistance electrical connection. With typical normal forces currently below 100 grams, the interactions between the major contact design parameters must be known to optimize the design of reliable, cost-effective connectors.

Research performed at the CALCE EPRC has focused on identifying the significant effects and interactions of the following electric contact design parameters: normal force, contact geometry, gold plating thickness, mixed flowing gas exposure, and wipe at t he contact interface on nickel- and gold-plated contact finishes. To collect the data necessary for this research, an automated contact resistance probe (ACRP) was developed. This instrument enables contact resistance measurements to be made on small anomalies on contact surfaces, such as corroded pore sites and dust pa rticles, with the help of video targeting algorithms. In addition to the CALCE EPRC core research, the ACRP has been used in contract projects for AT&T Bell Laboratories and Medtest Systems.

Specific results of our research can be categorized into electrical contact to nickel surfaces, electrical contact to pore-corroded gold surfaces, characterization of the occurrence of corroded pores, and a simulation of making contact to a pore-corroded surface.

Electrical Contact to Nickel Surfaces
The effects of wipe and backwipe on nickel-plated contact surfaces exposed to the Battelle class II MFG

environment were examined. While nickel contact finishes generally do not have low contact resistance properties after exposure to corrosive environmen ts, the addition of small amounts of wipe significantly decreased the contact resistance. There appears to be a minimal length of wipe after which little decrease in resistance was noted. Wipes in the opposite direction (backwipe) were shown to further de crease the contact resistance. The beneficial effect of backwipe is of special interest since it has not been seen in softer contact materials such as copper and gold. These results indicate that for connectors that must employ a nickel contact finish, bo th wipe and backwipe should be incorporated into the design for reliable performance.

Electrical Contact to Pore Corroded Gold Surfaces

The prevalent form of contact corrosion in light industrial environments is pore corrosion, which causes discrete mounds of corrosion randomly distributed on the contact finish. Contact on or off of these corroded pore sites was found to be a very signifi cant variable affecting the contact resistance. Contact resistance measurements made in the "clean" area directly outside corroded pore sites produced contact resistance values only slightly higher than those from clean gold-plated coupons. Wipe in these areas reduced the contact resistance, but backwipe had no effect. Readings made just inside the edge of a corroded pore gave contact resistance measurements te ns to hundreds of milliohms higher than those on clean gold. Readings made in center areas of corroded pores produced very high contact resistance measurements, many of which were open circuit. Wipe and backwipe were not effective in reducing the contact resistance when the probe landed on corroded pore sites.

These results show that as long as electrical contact is not made on a corroded pore, the contact resistance will be low. Important design implications are that low contact resistance is independent of the gold-plating thickness and exposure to the corro sive environment, and that the overall reliability of the gold contact surface is significantly impacted by the size and number of corroded pores on the surface.

Porosity Characterization

Since the occurrence of pore corrosion has such a significant effect on the contact resistance properties of a gold-plated finish, a method of characterizing the corrosion is necessary. Current methods in industry typically employ counting schemes where t he number of corroded pores in a control area are tabulated. A more quantitative method of porosity characterization was developed by which the actual area of the finish covered by pore corrosion was measured using image processing hardware. Using this me thod, relationships were developed for the percent area covered by pore corrosion as a function of gold-plating thickness and MFG exposure time. A benefit of this approach is that not only is the severity of the pore corrosion determined, but the result c an be used to estimate the probability that contact would be made on or off a corroded pore site as a function of gold-plating thickness and MFG exposure time.

Contact Simulation

The results of the porosity evaluation and the contact resistance testing in both the on and off pore cases were combined to provide an estimate of the contact resistance of a pore-corroded gold surface. Monte Carlo techniques were used to simulate a "bli nd land" on a pore-corroded gold surface. The porosity characterization results were used to determine whether contact is made on or off a corroded pore site. The contact resistance was then estimated using proper test distribution, depending on the simul ation inputs. This algorithm was iterated until a stable profile was developed. In this manner, a simulation of contacting to pore-corroded gold contact-surfaces can be conducted with normal force, geometry, wipe, gold-plating thickness and MFG exposure t ime as inputs.

For more information, please contact Dr. Michael Pecht at (301) 405-5323 or e-mail at pecht@eng.umd.edu.

Release of New calcePWA 1.3 Software

The latest version of the CALCE EPRC "calcePWA" design assessment software for circuit card assemblies was released in April. The calcePWA toolset provides users the ability to model and analyze

circuit card assemblies under thermal and mechanical loads a s well as to perform physics-of-failure evaluations. This year, the physics-of-failure evaluation has been extended to include conductive filament formation. In addition, enhancements and updates have been included to improve fatigue analysis reports, lea d modeling capabilities, tabular views of material and component information, design locking, the HTML online help system, and advance editing capabilities for CCA modeling. Previously, it could import designs from Mentor's BoardStation and Protel's Adva nced PCB Design System; this year the import capability is being extended to include design files from the PADS PWB Layout System. In addition, the import method has been developed for design files from the RECAL/REDAC PCB system.

This new software has already seen action in a variety of systems. It has been used to evaluate circuit card assemblies for communication systems such as the Joint STARS Communication system, Smart-T Radio System, and the AVR system for the B2. It has bee n used to model cards in a variety of radar systems, as well as various avionics PWB cards for the F-22. Saturn Corporation has been using the software as a prescreen on the design and test of an instrument control cluster board for one of their new cars. The software is being used to evaluate three cards in the ARC-210 transceiver system developed by Collins Avionics and Communication Division, CALCE EPRC, and the U.S. Army. In addition, Texas Instruments has licensed portions of the software for usage i n their CARMA product, and also markets a commercialized CALCE version of C-CALCE. And finally, the U.S. Army AMSAA plans to use the software to evaluate a total of twelve CCAs, and Rockwell CSD is using the calcePWA toolset to redesign and qualify the BI U card for its high-frequency radio.

In addition to the calcePWA toolkit, CALCE EPRC is pleased to announce the beta release of calceCFD, a new software package capable of predicting thermal, fluid flow, and pressure fields within a convection-cooled three-dimensional rectangular enclosure. CalceCFD is a computational fluid dynamics (CFD) based algorithm particularly suited for thermal analysis of electrical/electronic enclosures. The calceCFD tool was developed under the direction of Dr. Yogi Joshi and was used this year by University of Ma ryland graduate students to model various electronic enclosures.

The calcePWA software is currently available to members of the CALCE EPRC. In addition, a portion of the software has been licensed to Texas Instruments for use in their CARMA product. For more information on the calcePWA software contact Dr. Michael Oste rman 301-405-8023, fax (301) 314-9269, or e-mail osterman@eng.umd.edu. For information about calce-CFD contact Dr. Yogi Joshi at (301) 405-5428. For information on the Texas Instruments CARMA and C-CALCE product co ntact Keith Janasek at (214) 997-5970.

New Equipment Acquisitions

CALCE has acquired new equipment to broaden our state-of-the-art capability.

1. An Isthmus Dynamic Hygro-thermal Mechanical Analyzer is used to conduct in-site measurements of the relative humidity and temperature dependence of mechanical properties of thin-film materials and the effect of these parameters on damage behavior under various environmental and loading conditions.
2. The Micro-Quad 8000 Fully Digital Microprocessor-based Infrared Moisture Analyzer allows sophisticated data manipulation, and an integral printer provides hard copy data. It also features an RS232C interface port and multiple LED displays.
3. The Electrical Test Equipment-Tektronix S-3270 128 pin digital electrical test equipment is capable of testing the functionality of TTL, ECL, CMOS devices, and microprocessors. Its DC capabilities range from 100V to 100mV and 450mA to a few nA.
4. The Keithley Electrometer/High Resistance Meter Model 6517 is able to perform leakage, breakdown, and resistance testing, as well as volume (ohm-cm) and surface resistivity (ohm/square) measurements on insulating materials.
5. The Keithley LCZ Meter Model 3322 provides precision component and circuit testing with test frequencies up to 100kHz.
6. The Dynamic Burn-in System is designed to test microprocessors and memories under dynamic

operational conditions. The system is configured to use fifty-two Universal burn-in boards and has the flexibility to dynamically exercise most devices without hardware changes.

Electronic Packaging Manufacturing Lab

The CALCE EPRC now has a full service manufacturing facility called the CALCE EPRC Electronic Packaging Manufacturing Lab. To process development and optimization in SMT manufacturing, our facility is conducting research and performing experiments on all electronic produc ts and their associated processes. With our fully equipped manufacturing lab we are equipped and staffed to engineer electronic products from concept through test. The lab is equipped to deposit solder paste by stencil, screen, or by syringe manually, sem i-automatically, or fully automatically. In addition, the lab is equipped for pick and place, reflow both automatically and manually, inspection, rework and repair, statistical process control, training in manufacturing processes, and a complete library o f electronic manufacturing supplemented by a decade of IPC specifications and standards.

For further information, contact either Dr. Abhijit Dasgupta at: telephone (301) 405-5251 or e-mail dasgupta@eng.umd.edu , or Ed Beatty at: telephone (301) 405-5231 or e-mail beatty@eng.umd.edu. Both can be reached by fax at (301) 314-9269.

Dr. Wataru Nakayama joins CALCE EPRC

Dr. Wataru Nakayama from the Tokyo Institute of Technology has joined the CALCE EPRC staff starting June 1996 as a Professor. He is internationally known in the area of electronic packaging, with technical expertise in the area of thermal management. Prio r to joining the Tokyo Institute of Technology, he spent more than twenty years with Hitachi, Ltd. Dr. Nakayama's experience in the industry, the university, and various international professional communities will add a new window for CALCE. He will revie w packaging practices currently employed by the industry, identify the needs for basic research, and coordinate them to effect their integration into the development of CALCE research programs. The ultimate objective of his work at CALCE is the establishm ent of rational thermal design criteria and thermal screening programs on the basis of the physics-of-failure approach. Besides his research and coordination works, he will also be involved in teaching several courses in the area of electronic packaging. For more information, please contact Dr. Wataru Nakayama at: telephone (301) 405-5306, fax (301) 314-9269, or e-mail: nakayama@eng.umd.edu.

MEMs-Based Packaging

The CALCE Electronic Packaging Manufacturing Lab has entered the field of MEMs-based electronic packaging. After the successful disposition of a conductive epoxy in .006" dots on four hundred micron pads, the manufacturing lab was chosen to assemble 30 MEMs-based ac celerometers for Optical E.T.C., Inc. of Huntsville, Alabama. Using the staff and equipment in the lab, thirty chip dies will be attached to thirty carriers using a conductive epoxy. Electrical performance will be observed during assembly. The assemblies will then be inspected. The packaging technique is unique and the manufacturing lab at CALCE is equipped and staffed to assemble, manufacture, inspect, and test the devices for product assurance and lifetime reliability.

Solder Paste Process Control

The CALCE Electronic Packaging Manufacturing Lab is now testing solder pastes that meet and exceed IPC's ANSI/J-STD-005 requirements. The lab has teamed with Marquette University and the California Polytechnic University, San Luis Obispo to do this u sing AC impedance spectroscopy. The EMPF of Indianapolis, Indiana is donating the use of an IS4000 to the Electronic Packaging Manufacturing Lab in order to do this.

Daewoo Scholars Visit CALCE

Daewoo and CALCE have developed a strong working relationship. Part of this relationship has manifested itself with the visit to CALCE of research engineer Jin Woo Kim from Daewoo Electronics, one of the largest electronics companies in South Korea. Mr. K im will spend six months at CALCE working on the design, manufacture, and reliability of electronic components. When he leaves, he will be replaced by another research engineer from Daewoo, Hee Jin Lee. Ms. Lee will also spend six months at CALCE, pursuin g the same line of research as Kim. This type of effort provides valuable experience to the two researchers, strengthens the working relationship between Daewoo and CALCE, allows mutually beneficial research to be done at the CALCE facility, and provides CALCE personnel with valuable experience from working with two of Daewoo's research engineers. This joint operation is just a furtherance of CALCE's desired goal to work with its member companies to further their research and development goals.

CALCE Students' Summer Cooperative Projects

Three CALCE EPRC students and member companies have spent a portion of their summer together. Jill Jordan, Prateek Dujari, and Damian Searls have worked on a regular, full-time basis for Honeywell, Eldec, and Texas Instruments, respectively. Each student has worked on a variety of projects. Jill has conducted temperature tests on a digital printed circuit and power supply board, worked on developing a plastic off-the-shelf connector, organized efforts with various companies to get electronics parts teste d and to develop a publication on screening techniques, and worked on a major problem concerning stress induced board-bending. Prateek is working on the development of a methodology to handle the accelerated stress testing of electronic systems. He is als o working on developing one for reliability enhancement testing. Damian is developing techniques to use CADMP methods in the virtual qualification of parts and the assessment of the reliability of plastic encapsulated microcircuits.

During the school semester these three students had already been working on member projects for these companies. This summer experience will provide both them and the companies an excellent opportunity to get to know each other better, possibly leading to future job opportunities.

Directed Studies in Critical Technologies Award

A fully funded government scholarship has been awarded to Leon Lantz to study key issues associated with the commercial insertion of plastic encapsulated microcircuits into high- reliability applications. Leon will be measuring ion diffusion rates in comm ercial molding compounds and assessing the correlation between ion diffusion rates and corrosion-related failures in PEMs.

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CALCE EPRC AND MEMBER COMPANY SHARE UPRATING SUCCESS

The number of commercial microcircuits used at temperatures outside the manufacturer's recommended temperature range is expected to increase over the next few years as the availability of MIL-STD parts continues to shrink. As a result of this increasing trend to use commercial components in harsher environments, the CALCE EPRC has instituted a core research project to develop a generic methodology for qualifying commercial components for use outside their normal temperature ranges. This methodology will address issues of device performance, reliability, and vendor selection as well as practical legal concerns.

The potential for success from this research effort was recently realized by AlliedSignal, a CALCE EPRC member company, which considered substituting a commercial avionics microcontroller for a hermetic ceramic one. The commercial version of the component is readily available at $19/part. The MIL-STD hermetic packaged version must be specially made at a cost exceeding $560/part - thirty times more.

In order to make this substitution, AlliedSignal and the CALCE EPRC defined a program for qualifying an industrial temperature range (-40C to 85C) microcontroller for use from -55C to 125C. This program consisted of both performance and durability testing. It has also leveraged off other CALCE EPRC core research efforts to develop criteria for manufacturer parts assessment, to determine the potential failure mechanisms of PEMs at low temperatures, and to characterize the growth of delamination and cracking in PEMs subjected to temperature cycling to extremely low temperatures (< -55C).

Testing conducted on a hundred microcontrollers indicated that the device would operate from -100C to 160C. Full parametric testing indicated the device would remain within the manufacturer's electrical performance specifications from -70C to 150C. In addition, reliability degradation was not observed in any of the samples after exposure to the durability tests. Contact: Dr. P. McCluskey at mcclupa@eng.umd.edu.

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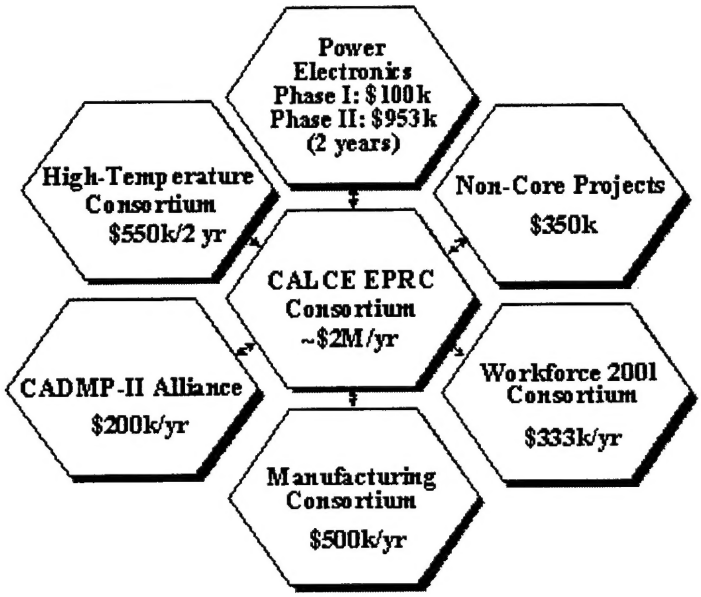

The CALCE Electronic Packaging Research Center (EPRC) at the University of Maryland is a research, technology transfer, and educational organization that provides a resource base to support the development of competitive electronic products and systems in a timely manner. The Center receives the majority of its support from seven sources, which are shown above and explained below.

- **CALCE EPRC Consortium** - The Consortium consists of thirty-five organizations that support and share all the results of CALCE core proprietary projects. Key projects include parts/supplier selection and management, commercial insertion into high-reliability applications, using components outside their rated limits, physics-of-failure modeling, design guidelines, accelerated testing, and thermal management.
- **Power Electronics Building Blocks** - The Office of Naval Research supports this effort to develop smart power electronics and advanced packaging technologies leading to intelligent, programmable, multifunctional, modularized power systems capable of controlling up to 250 kW. These systems will be used in surface and underwater vessels and in commercial vehicles. CALCE is responsible for developing packaging and reliability assessment software to make these systems a reality.
- **High Temperature Electronics Consortium** - A 14-member DARPA consortium supports the development at CALCE EPRC of distributed control system that can operate without cooling. These are essential to next generation automotive and aerospace systems because of their potential to reduce the cost, size, and weight of electronics systems while increasing performance, reliability, and maintainability. The high-temperature electronics work dovetails with (or focuses on) the CADMP-II research described below.
- **CADMP-II Alliance** - This consortium of component manufacturers and users is dedicated to enhancing physics-of-failure reliability assessment software at the component, MCM, and hybrid packaging levels. Current research includes developing an extensive electronic materials database, a failure mechanism database, and advanced methods for reliability assessment.

- **Manufacturing Consortium** - This consortium is a DARPA supported program to improve manufacturing competitiveness through innovative education, and courseware development. Manufacturing Consortium is integrating novel teaching methods and tools to prepare students and engineers for 21st century design and manufacturing.
- **Workforce 2001** - This program is developing an educational curriculum focused on life cycle design, manufacturing, and usage of electronic systems and products. The program involves transferring expertise in critical 21st century electronics manufacturing technologies to graduate students and engineering and technical professionals through workshops, books, regular and short courses, videos, and websites. This has resulted in 12 books, including one on high-temperature electronics and a book series on the Southeast Asian electronics industry.
- **Non-core projects** - CALCE EPRC remains committed to assisting companies in focused, proprietary research and development activities through non-core research projects.

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